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ECE

1. Integrated circuits

Introduction :-

The Integrated circuit (or) Ic is a miniature, Low cost electronic circuit consisting of active and passive elements and they are fabricated on a single silicon chip is called "Integrated circuits".

The main Semiconductor material utilized is Silicon, but for special applications, gallium arsenide and other semiconductor materials also be utilized.

Advantages of Ic's :-

1. Small Size
2. Low cost
3. Less weight
4. Low supply voltages
5. Low Power consumption
6. Fast speed
7. Highly reliable

Types of Ic's :- There are 2 types

1. Linear Ics
2. Digital Ics

1. Linear Ics (or) Analog Ics :-

The term linear used since output value is a linear function of Input.

Ex :- Filters, modulators, Amplifiers like Inverting and Non Inverting.

→ These Ics mostly used in audio and radio frequency applications.

2. Digital Ics :-

These Ics concerned with 2 levels either 1 (or) 0.

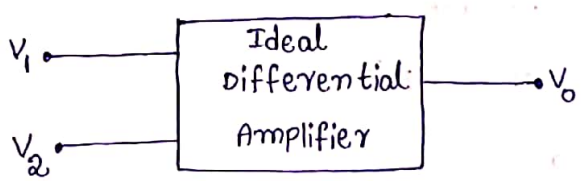
Low level signal send to a Input, the output should be zero.

High level signal send to a Input, the output should be '1'.

Ex :- counters, Gates, mux etc...

→ These Ics mostly used in consumer electronics.

Differential Amplifier :-



V_1, V_2 → Two Input signals

V_o → output signal

In Ideal differential Amplifier, output voltage V_o is proportional to the difference between 2 Input signals.

$$V_o \propto (V_1 - V_2)$$

$$\boxed{V_o = A_d(V_1 - V_2)}$$

Differential gain (A_d) :-

$$V_0 = A_d (V_1 - V_2)$$

where $A_d \rightarrow$ proportionality constant.

A_d is the gain.

consider $V_1 - V_2 = V_d$

$$\Rightarrow V_0 = A_d V_d \Rightarrow \boxed{A_d = \frac{V_0}{V_d}}$$

common mode gain (A_c) :-

If we apply 2 Input voltages are equal (common) i.e $V_1 = V_2$ then $V_0 = A_d (V_1 - V_2)$

$$= A_d (V_1 - V_1) = 0 \quad \Rightarrow V_0 = 0$$

But the output voltage of the practical differential amplifier not only depends on the difference voltage but also depends on the average of 2 Inputs.

Such an average level of 2 Input signals is called common mode signal (V_c).

$$\boxed{V_c = \frac{V_1 + V_2}{2}}$$

Practically, differential amplifier produces the output voltage proportional to common mode signals,

$$\boxed{V_0 = A_c V_c}$$

Total output of any differential amplifier can be expressed as,

$$\boxed{V_0 = A_d V_d + A_c V_c}$$

Common mode Rejection Ratio (CMRR) :-

The ability of a differential amplifier to reject a common mode signal is expressed by a ratio called common mode rejection ratio.

It is defined as the ratio of differential gain A_d to the common mode gain A_c.

$$CMRR = \frac{|A_d|}{|A_c|}$$

For, $A_d \rightarrow$ Large value, $A_c \rightarrow$ Small value

$CMRR \rightarrow$ High value.

In terms of dB, $CMRR \text{ in } dB = 20 \log \frac{|A_d|}{|A_c|}$ dB

output voltage expressed in terms of CMRR as

$$V_o = A_d V_d + A_c V_c = A_d V_d \left[1 + \frac{A_c V_c}{A_d V_d} \right]$$

$$= A_d V_d \left[1 + \frac{1}{\left(\frac{A_d}{A_c}\right)} \cdot \frac{V_c}{V_d} \right]$$

$$V_o = A_d V_d \left[1 + \frac{1}{CMRR} \cdot \frac{V_c}{V_d} \right]$$

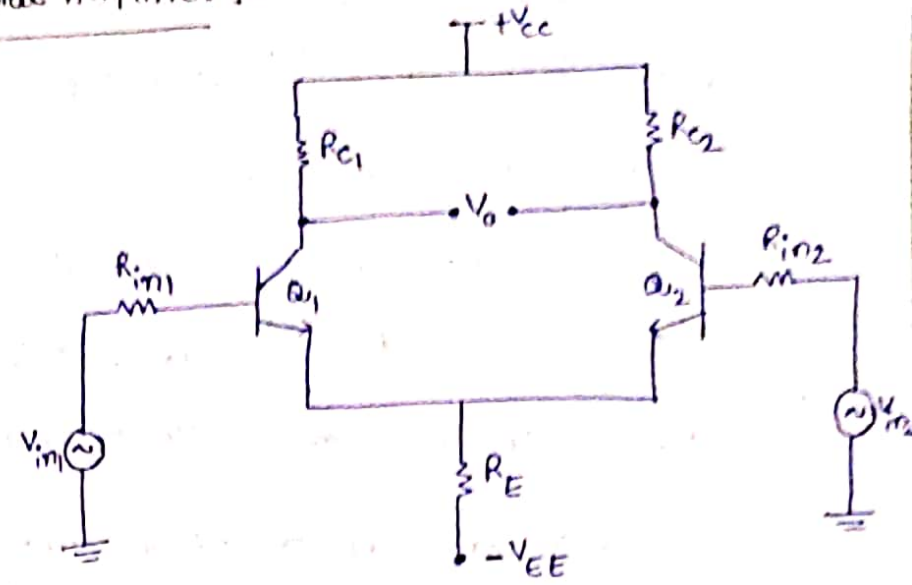
Feadures of differential Amplifier :-

There are various features,

1. High differential voltage gain
2. Low common mode gain
3. High CMRR
4. High Input Impedance
5. Low output Impedance
6. Low offset voltages and currents.

operation of differential Amplifier :-

circuit diagram :-



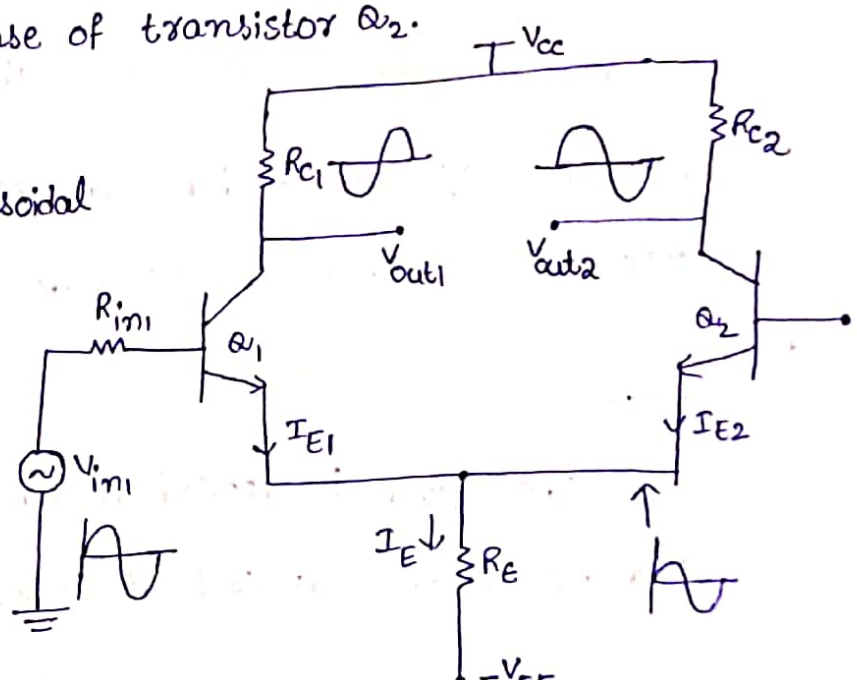
In this diagram, there are 2 Inputs, 2 outputs are used.

→ Here, 2 separate transistors Q_1, Q_2 are used and apply 2 Inputs at base of both transistor.

→ 2 separate transistors having similar characteristics ideally, common emitter resistor R_E, positive supply voltage V_{cc} and Negative supply V_{EE}.

working :-

case ① :- A signal is applied at base of transistor Q_1 and no signal is applied at base of transistor Q_2.



The Input signal sinusoidal applied at base of the transistor Q_1.

First, The positive half cycle is applied at base of Q_1, the transistor ON.

→ If the transistor turns 'ON' there will be ~~more~~ voltage drop across R_{C_1} will be ~~more~~ resulting the collector of Q_1 to be less positive. and current flows through the circuit.

→ The -ve half cycle is applied at base of transistor Q_1, the transistor turned OFF, resulting in less voltage drop across R_{C_1}, No current flows through the circuit.

→ In this way, an Inverted output appears at collector of Q_1, by appling signal at Input of Q_1.

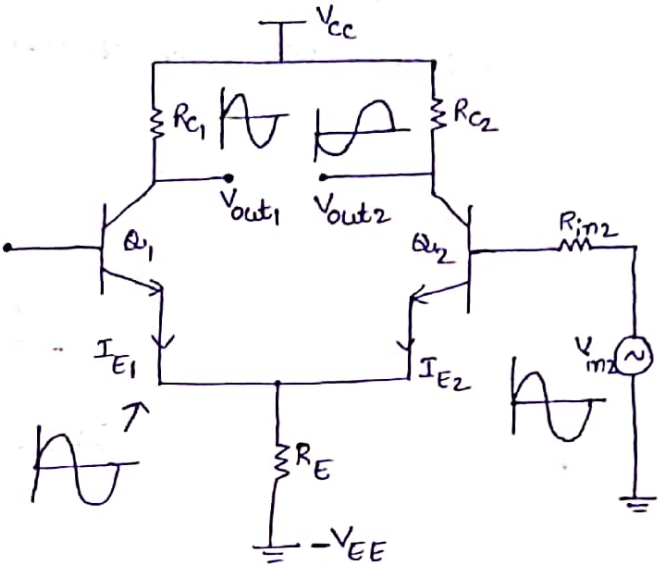
→ At the time when Q_1 gets ON by +ve half cycle of Input, the current through R_E will Increase. So, Voltage drop at R_E will be more causing the emitters of both transistors go in +ve direction.

→ No Input is applied at base of transistor Q_2 (zero Input) So transistor Q_2 turned OFF. There is no voltage drop across R_{C_1} and No current flows through the circuit.

→ In this way, we will have a non-Inverting output at collector of Q_2 for +ve Input at base of Q_1.

case ②:-

The signal is applied at base of transistor Q_2 and tra no Input is applied at transistor Q_1 base terminal.



In this case, first the +ve half cycle is applied to base of transistor Q_2, transistor ON. there will be voltage drop across R_{C_2} and current flows through it.

second, The -ve half cycle is applied at Q_2, transistor turned OFF. so, there is no voltage drop across R_{C_2} and no current flows through it.

So, there will be Inverted output at R_{C_2}.

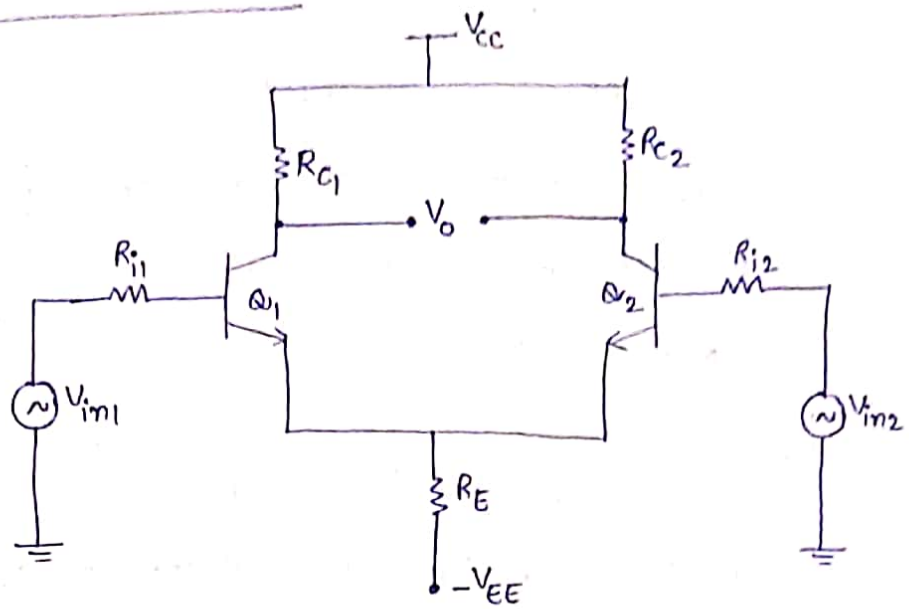
→ No Input is applied at base of transistor Q_1, so the transistor turned OFF, No voltage drop across R_{C_1} so the output across R_{C_1} will be Non-Inverted output.

Differential Amplifier configurations :-

Depending upon Input and output terminals of differential Amplifier, there are 4 configurations.

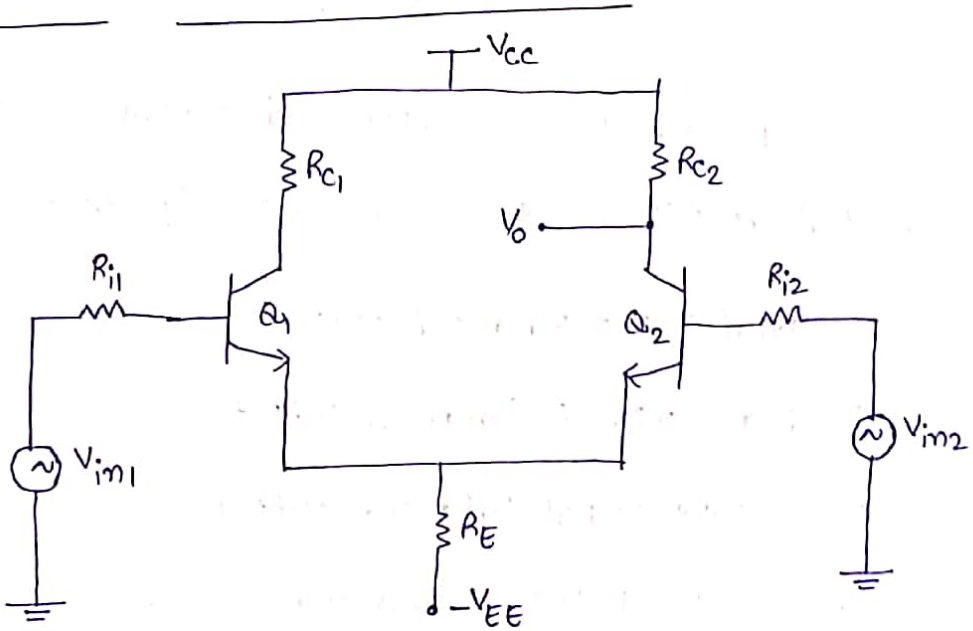
1. Dual Input Balanced output
2. Dual Input unbalanced output
3. Single Input balanced output
4. Single Input unbalanced output

1. Dual Input balanced output (DIBO) :-



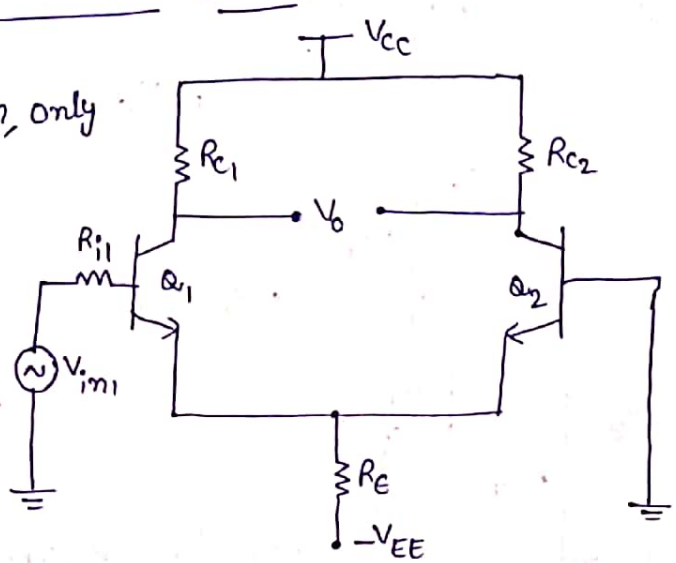
In this configuration, two Inputs are applied at base of transistor Q_1, Q_2 and output is taken between 2 collector terminals so, this configuration called as "Dual Input balanced output" (or) Dual Input double ended output (or) floating output (or) symmetrical differential Amplifier.

2. Dual Input unbalanced output (DIUBO) :-



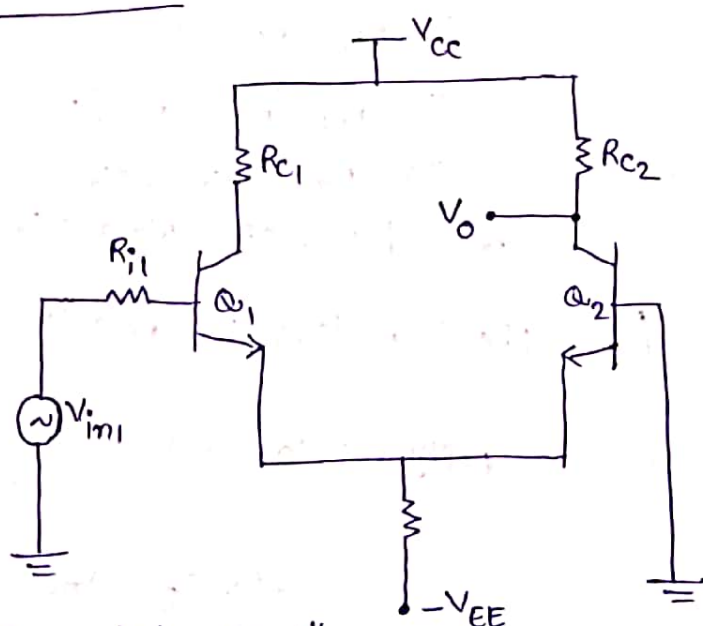
In this configuration, 2 Inputs applied at base of transistor Q_1, Q_2 and output is taken between one collector terminal is called "dual Input unbalanced output" (or) "Dual Input single ended output."

3. single Input balanced output (SIBO):-



In this configuration, only one Input is applied at base of transistor Q_1, and output is taken between 2 collector terminals is called "single Input balanced output" (or) "single Input double ended output".

4. single Input unbalanced output (SIUBO):-

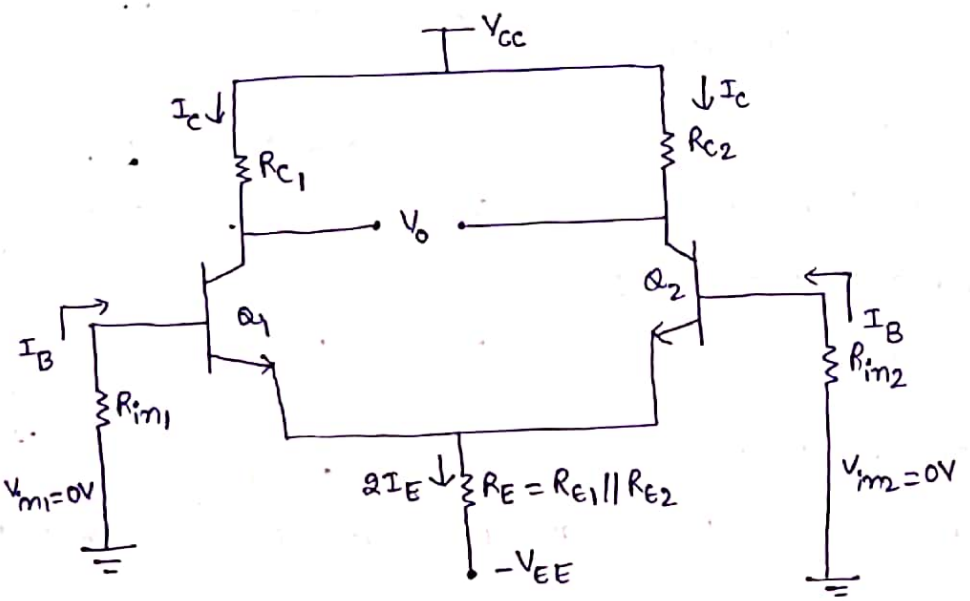


In this configuration, only one Input is applied at base of transistor Q_1 and output is taken at only one collector terminal is called "single Input unbalanced output" (or) "single Input Single ended output".

D.C Analysis of differential Amplifier :-

To determine the operating point values i.e I_{CQ} and V_{CEQ} for the differential Amplifier.

The DC equivalent circuit can be obtained by reducing the Input A.C signals to zero.



→ Both transistors are matched transistors i.e symmetrical,

i) $R_{C_1} = R_{C2} = R_C$

ii) $R_{E1} = R_{E2} = R_E$ ($\because R_E = R_{E1} \| R_{E2}$)

iii) $R_{in_1} = R_{in2} = R_{in}$

To find out operating points I_{CQ} and V_{CEQ}, for any one of the transistors. same is applicable for other transistor.

Apply KVL to Base-emitter loop

$$-R_{in} I_B - V_{BE} - R_E (2I_E) - (-V_{EE}) = 0$$

$$-R_{in} I_B - V_{BE} - 2I_E R_E + V_{EE} = 0 \quad \text{— ①}$$

we know that,

$$\beta_{dc} = \frac{I_E}{I_B} \Rightarrow I_B = \frac{I_E}{\beta_{dc}} \quad -(2)$$

Substitute eqn (2) in eqn (1),

$$-R_{in} I_B - V_{BE} - 2R_E I_E + V_{EE} = 0$$

$$\Rightarrow V_{EE} - V_{BE} = R_{in} I_B + 2R_E I_E$$

$$\Rightarrow V_{EE} - V_{BE} = R_{in}\left(\frac{I_E}{\beta_{dc}}\right) + 2R_E I_E$$

$$= I_E\left(\frac{R_{in}}{\beta_{dc}} + 2R_E\right)$$

$$\Rightarrow I_E = \frac{V_{EE} - V_{BE}}{\left(\frac{R_{in}}{\beta_{dc}}\right) + 2R_E}$$

where, $V_{BE} = 0.6$ to 0.7 for Si

$= 0.2$ for Ge.

consider $\frac{R_{in}}{\beta_{dc}} << 2R_E$

$$\Rightarrow I_E = \frac{V_{EE} - V_{BE}}{2R_E} \quad -(3)$$

w.k.t $I_E \approx I_C$

$$\Rightarrow \boxed{I_{C_Q} = \frac{V_{EE} - V_{BE}}{2R_E}} \quad -(4)$$

Determine V_{CEQ} :-

collector voltage of Q_1 as

$$V_C = V_{CC} - I_C R_C \quad -(5) \qquad (\because V_{CC} = I_C R_C + V_C \Rightarrow V_C = -I_C R_C + V_{CC})$$

collector-to-emitter voltage is

$$V_{CE} = V_C - V_E \quad \text{—⑥}$$

Substitute eq ⑤ in eq ⑥,

$$\Rightarrow V_{CE} = V_{CC} - I_C R_C - V_E$$

$$= V_{CC} - I_C R_C - (-V_{BE}) \qquad (\because V_E = V_{BE})$$

$$\boxed{V_{CE} = V_{CC} + V_{BE} - I_C R_C}$$

(or)

$$\boxed{V_{CEQ} = V_{CC} + V_{BE} - I_{CQ} R_C} \quad \text{—⑦}$$

Note :- The D.C Analysis expressions for I_{CQ} and V_{CEQ} remain same for all the four differential amplifier configurations.

A.C Analysis :-

To perform A.C Analysis to derive the expressions for voltage gain (A_d), Input resistance (R_i) and output resistance (R_o).

Assumptions:-

i) set the D.C voltages $+V_{CC}$ and $-V_{EE} = 0$

ii) substitute the small signal T equivalent models for the transistors.

1. Dual Input balanced output differential Amplifier :-

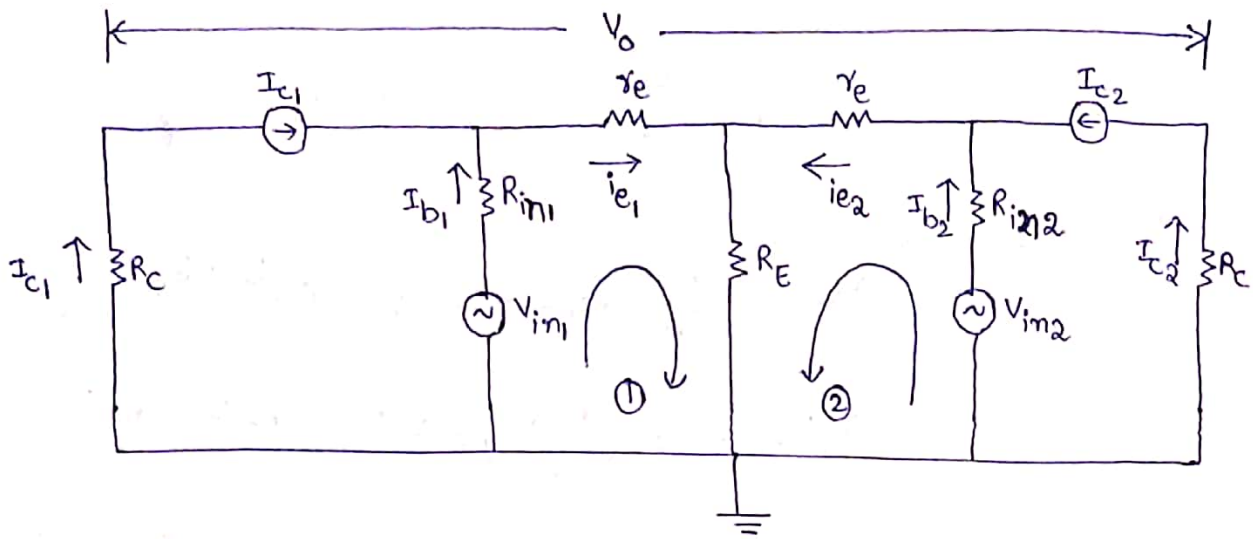
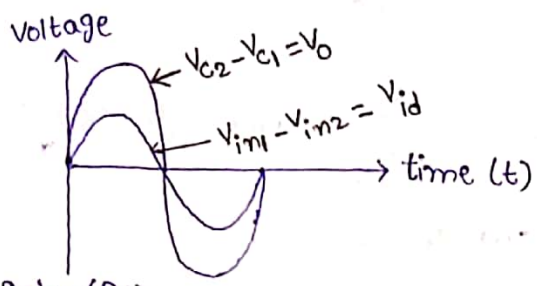


Fig:- A.c equivalent circuit for Dual Input balanced output



i) Voltage gain (A_d)

KVL for loop 1 and 2

$$V_{in1} - I_{b1} R_{in1} - r_e i_{e1} - R_E (i_{e1} + i_{e2}) = 0 \quad \text{— ①}$$

$$V_{in2} - I_{b2} R_{in2} - r_e i_{e2} - R_E (i_{e1} + i_{e2}) = 0 \quad \text{— ②}$$

w.k.t $\beta_{ac} = \frac{i_e}{i_b} \Rightarrow i_b = \frac{i_e}{\beta_{ac}}$

So $i_{b1} = \frac{i_{e1}}{\beta_{ac}}$ — ③ , $i_{b2} = \frac{i_{e2}}{\beta_{ac}}$ — ④

Substitute eq ③, ④ in eq ①, ②

eq① $\Rightarrow V_{in1} - \left(\frac{i_{e1}}{\beta_{ac}}\right) R_{in1} - r_e i_{e1} - R_E (i_{e1} + i_{e2}) = 0$

$\Rightarrow V_{in1} = \left(\frac{i_{e1}}{\beta_{ac}}\right) R_{in1} + r_e i_{e1} + R_E (i_{e1} + i_{e2})$

$$\Rightarrow V_{in_1} = ie_1\left(\frac{R_{in_1}}{\beta_{ac}}\right) + r_e\, ie_1 + R_E\, ie_1 + R_E\, ie_2$$

$$= ie_1\left(\frac{R_{in_1}}{\beta_{ac}} + r_e + R_E\right) + R_E\, ie_2 \quad \text{——⑤}$$

eq② ⇒

$$V_{in_2} - \left(\frac{ie_2}{\beta_{ac}}\right) R_{in_2} = r_e\, ie_2 - R_E(ie_1 + ie_2)$$

$$\Rightarrow V_{in_2} = ie_2\left(\frac{R_{in_2}}{\beta_{ac}}\right) + r_e\, ie_2 + R_E\, ie_1 + R_E\, ie_2$$

$$= ie_2\left(\frac{R_{in_2}}{\beta_{ac}} + r_e + R_E\right) + R_E\, ie_1 \quad \text{——⑥}$$

consider $(r_e + R_E) >> \frac{R_{in_1}}{\beta_{ac}}$ and $(r_e + R_E) >> \frac{R_{in_2}}{\beta_{ac}}$ then

eq⑤, eq⑥ changes to

$$V_{in_1} = ie_1(r_e + R_E) + R_E\, ie_2 \quad \text{——⑦}$$

$$V_{in_2} = ie_2(r_e + R_E) + R_E\, ie_1 \quad \text{——⑧}$$

eq⑦, eq⑧ can be written as

$$(r_e + R_E)\, ie_1 + (R_E)\, ie_2 = V_{in_1}$$

$$(R_E)\, ie_1 + (r_e + R_E)\, ie_2 = V_{in_2}$$

Apply cramers rule

$$ie_1 = \frac{\begin{vmatrix} V_{in_1} & R_E \\ V_{in_2} & r_e + R_E \end{vmatrix}}{\begin{vmatrix} r_e + R_E & R_E \\ R_E & r_e + R_E \end{vmatrix}} \quad \text{and} \quad ie_2 = \frac{\begin{vmatrix} r_e + R_E & V_{in_1} \\ R_E & V_{in_2} \end{vmatrix}}{\begin{vmatrix} r_e + R_E & R_E \\ R_E & r_e + R_E \end{vmatrix}}$$

$$ie_1 = \frac{(r_e + R_E)V_{in1} - R_E V_{in2}}{(r_e + R_E)^2 - R_E^2} \quad \text{—(9)}, \qquad ie_2 = \frac{(r_e + R_E)V_{in2} - R_E V_{in1}}{(r_e + R_E)^2 - R_E^2} \quad \text{—(10)}$$

The output voltage $V_o = V_{c2} - V_{c1}$

$$= -R_c ic_2 - (-R_c ic_1)$$

$$= -R_c ic_2 + R_c ic_1$$

w.k.t $I_c \simeq I_E$, $V_o = -R_c ie_2 + R_c ie_1$ —(11)

substitute eq(9), (10) in eq(11)

$$\Rightarrow V_o = -R_c \left[\frac{(r_e + R_E)V_{in2} - R_E V_{in1}}{(r_e + R_E)^2 - R_E^2} \right] + R_c \left[\frac{(r_e + R_E)V_{in1} - R_E V_{in2}}{(r_e + R_E)^2 - R_E^2} \right]$$

$$= R_c \left[\frac{(r_e + R_E)V_{in1} - R_E V_{in2} - (r_e + R_E)V_{in2} + R_E V_{in1}}{(r_e + R_E)^2 - R_E^2} \right]$$

$$= R_c \left[\frac{(r_e + R_E)(V_{in1} - V_{in2}) + R_E(V_{in1} - V_{in2})}{r_e^2 + R_E^2 + 2 r_e R_E - R_E^2} \right]$$

$$= R_c \left[\frac{(r_e + R_E + R_E)(V_{in1} - V_{in2})}{r_e(r_e + 2R_E)} \right]$$

$$V_o = R_c \left[\frac{(r_e + 2R_E)(V_{id})}{r_e(r_e + 2R_E)} \right] \qquad (\because V_{in1} - V_{in2} = V_{id})$$

$$V_o = \frac{R_c}{r_e} V_{id} \Rightarrow \frac{V_o}{V_{id}} = \frac{R_c}{r_e} \qquad (\because \frac{V_o}{V_{id}} = A_d)$$

$$\Rightarrow \boxed{A_d = \frac{R_c}{r_e}}$$

ii) Input resistance (R_i):-

$$R_{i_1} = \left.\frac{V_{in_1}}{I_{b_1}}\right|_{V_{in_2}=0} \quad -①$$

$$R_{i_2} = \left.\frac{V_{in_2}}{I_{b_2}}\right|_{V_{in_1}=0} \quad -①$$

w.k.t $i_{b_1} = \frac{i_{e_1}}{\beta_{ac}}$ $-②$

$i_{b_2} = \frac{i_{e_2}}{\beta_{ac}}$ $-②$

substitute eq② in eq①

$$R_{i_1} = \left.\frac{V_{in_1}}{i_{e_1}/\beta_{ac}}\right|_{V_{in_2}=0} \quad -③$$

$$R_{i_2} = \left.\frac{V_{in_2}}{\frac{i_{e_2}}{\beta_{ac}}}\right|_{V_{in_1}=0} \quad -③$$

substitute i_{e_1}, i_{e_2} values

$$R_{i_1} = \left.\frac{V_{in_1}\beta_{ac}}{\frac{(r_e+R_E)V_{in_1} - R_E V_{in_2}}{(r_e+R_E)^2-(R_E)^2}}\right|_{V_{in_2}=0}$$

$$R_{i_2} = \left.\frac{V_{in_2}\beta_{ac}}{\frac{(r_e+R_E)V_{in_2} - R_E V_{in_1}}{(r_e+R_E)^2-(R_E)^2}}\right|_{V_{in_1}=0}$$

$$= \frac{V_{in_1}\beta_{ac}}{\frac{(r_e+R_E)V_{in_1} - R_E(0)}{r_e^2+R_E^2+2R_E r_e - R_E^2}}$$

$$= \frac{V_{in_2}\beta_{ac}}{\frac{(r_e+R_E)V_{in_2} - R_E(0)}{r_e^2+R_E^2+2r_e R_E - R_E^2}}$$

$$= \frac{V_{in_1}\beta_{ac}}{\frac{(r_e+R_E)V_{in_1}}{r_e(r_e+2R_E)}}$$

$$= \frac{V_{in_2}\beta_{ac}}{\frac{(r_e+R_E)V_{in_2}}{r_e(r_e+2R_E)}}$$

$$= \frac{\beta_{ac} r_e (r_e+2R_E)}{r_e+R_E}$$

$$= \frac{\beta_{ac} r_e (r_e+2R_E)}{r_e+R_E}$$

$R_E >> r_e$

$\Rightarrow R_{i1} = \dfrac{\beta_{ac} r_e (2R_E)}{R_E}$

$\Rightarrow \boxed{R_{i1} = 2\beta_{ac} r_e}$

$R_C >> r_e$

$\Rightarrow R_{i2} = \dfrac{\beta_{ac} r_e (2R_C)}{R_E}$

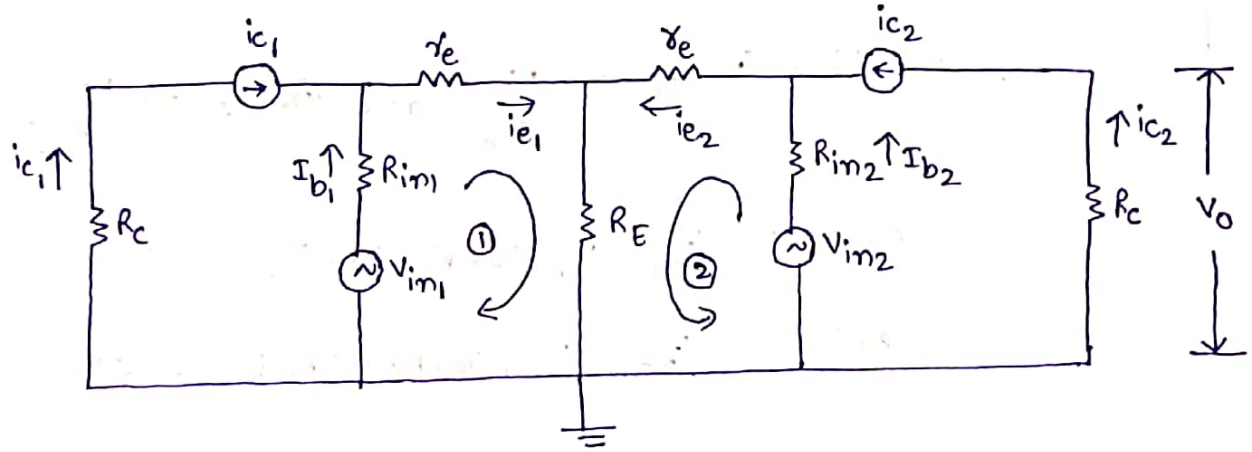
$\Rightarrow \boxed{R_{i2} = 2\beta_{ac} r_e}$

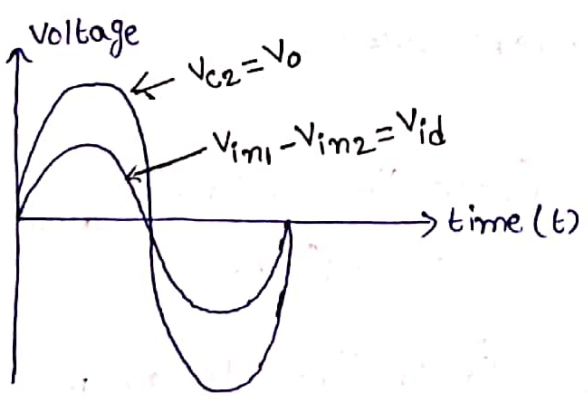
iii) output resistance :-

In Dual Input balanced output configuration output is taken between 2 collector terminals i.e

$R_{out1} = R_{out2} = R_C$ (or) $R_{O1} = R_{O2} = R_C$

2. Dual Input unbalanced output differential Amplifier :-





i) Voltage gain (A_d) :-

Apply KVL to Loop ① & ②

$$V_{in_1} - I_{b1} R_{in_1} - r_e i_{e_1} - R_E (i_{e_1} + i_{e_2}) = 0 \quad \text{—①}$$

$$V_{in_2} - I_{b2} R_{in_2} - r_e i_{e_2} - R_E (i_{e_1} + i_{e_2}) = 0 \quad \text{—②}$$

w.k.T $I_{b_1} = \frac{i_{e_1}}{\beta_{ac}}$, $I_{b_2} = \frac{i_{e_2}}{\beta_{ac}}$

substitute i_{b_1}, i_{b_2} values in eq ①, ②

from eq ①, $V_{in_1} = \frac{i_{e_1}}{\beta_{ac}} R_{in_1} + r_e i_{e_1} + R_E i_{e_1} + R_E i_{e_2}$

$$= i_{e_1} \left(\frac{R_{in_1}}{\beta_{ac}} + r_e + R_E \right) + R_E i_{e_2} \quad \text{—③}$$

eq ② $\Rightarrow$ $V_{in_2} = i_{e_2} \left(\frac{R_{in_2}}{\beta_{ac}} + r_e + R_E \right) + R_E i_{e_1}$ —④

consider $(r_e + R_E) >> \frac{R_{in_1}}{\beta_{ac}}$ and $(r_e + R_E) >> \frac{R_{in_2}}{\beta_{ac}}$ then

eq ③ $\Rightarrow$ $V_{in_1} = i_{e_1} (r_e + R_E) + R_E i_{e_2}$ —⑤

eq ④ $\Rightarrow$ $V_{in_2} = i_{e_2} (r_e + R_E) + R_E i_{e_1}$ —⑥

Apply crammers rule :-

$$i_{e_1} = \frac{(r_e + R_E) V_{in_1} - R_E V_{in_2}}{(r_e + R_E)^2 - R_E^2} \quad \text{and}$$

$$i_{e_2} = \frac{(r_e + R_E) V_{in_2} - R_E V_{in_1}}{(r_e + R_E)^2 - R_E^2}$$

The output voltage, $V_o = V_{c2}$

$= -i_{c_2} R_{c_2} = -i_{e_2} R_{c_2}$ $(\because i_c = i_e,\ R_{c_2} = R_c)$

$V_o = -R_c i_{e_2}$

$$= -R_c \left[\frac{(r_e + R_E) V_{in_2} - R_E V_{in_1}}{(r_e + R_E)^2 - R_E^2} \right]$$

$$= R_c \left[\frac{R_E V_{in_1} - (r_e + R_E) V_{in_2}}{r_e^2 + R_E^2 + 2 r_e R_E - R_E^2} \right]$$

$$= R_c \left[\frac{R_E V_{in_1} - (r_e + R_E) V_{in_2}}{r_e (r_e + 2R_E)} \right]$$

$$= R_c \left[\frac{R_E (V_{in_1} - V_{in_2})}{r_e (2R_E)} \right] \quad (\because R_E >> r_e)$$

$$V_o = R_c \left[\frac{V_{id}}{2 r_e} \right] \quad (\because V_{in_1} - V_{in_2} = V_{id})$$

$$\Rightarrow \frac{V_o}{V_{id}} = \frac{R_c}{2 r_e} \Rightarrow \boxed{A_d = \frac{R_c}{2 r_e}}$$

The voltage gain is half the gain of dual Input, balanced output differential amplifier.

ii) Input resistance :-

$$\boxed{R_{i_1} = R_{i_2} = 2 R_{ac} r_e}$$

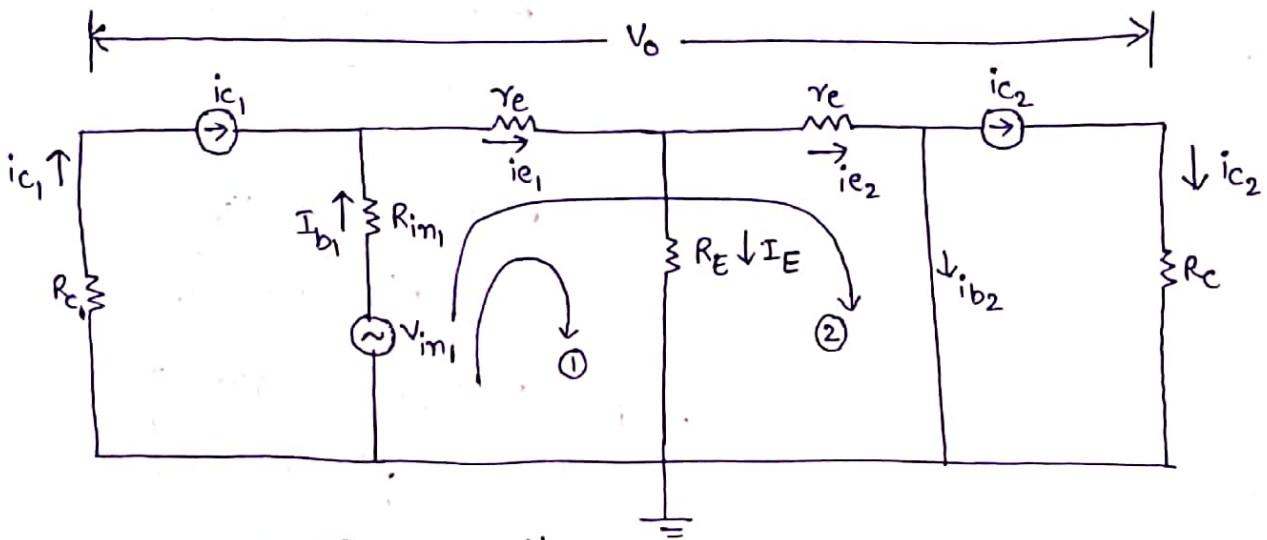
(∵ Procedure is same as Dual Input balanced Output - Input resistance)

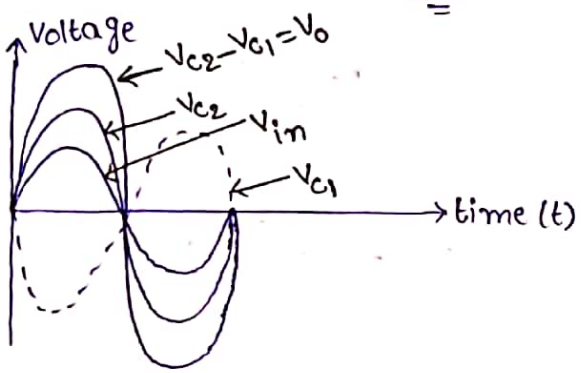
iii) output resistance :- In this configuration output is taken between one collector terminal

i.e $\boxed{R_{o_2} = R_c}$

3. Single Input balanced output differential Amplifier :-

In this configuration, Input is applied to base of transistor Q_1 and output is measured between 2 collector terminals.





i) Voltage gain (A_d) :-

Apply KVL to Loop ①, Loop ②

$$V_{in} - I_{b_1} R_{in_1} - r_e i_{e_1} - R_E I_E = 0 \quad \text{—— ①}$$

$$V_{in} - I_{b_1} R_{in_1} - r_e i_{e_1} - r_e i_{e_2} = 0 \quad \text{— ②}$$

w.k.T $I_{b_1} = \frac{i_{e_1}}{\beta_{ac}}$, $I_{b_2} = \frac{i_{e_2}}{\beta_{ac}}$

Substitute I_{b_1}, I_{b_2} in eq ①, ②

from eq①,

$$V_{in} - \left(\frac{i_{e_1}}{\beta_{ac}}\right) R_{in_1} - r_e i_{e_1} - R_E (i_{e_1} - i_{e_2}) = 0 \qquad (\because I_E = i_{e_1} - i_{e_2})$$

$$\Rightarrow V_{in} = \frac{R_{in_1}}{\beta_{ac}} i_{e_1} + r_e i_{e_1} + R_E i_{e_1} - R_E i_{e_2}$$

$$= i_{e_1}\left(\frac{R_{in_1}}{\beta_{ac}} + r_e + R_E\right) - R_E i_{e_2} \qquad (\because (r_e + R_E) >> \frac{R_{in_1}}{\beta_{ac}})$$

$$V_{in} = i_{e_1}(r_e + R_E) - R_E (i_{e_2}) \quad \text{——} ③$$

from eq②,

$$V_{in} = \left(\frac{i_{e_1}}{\beta_{ac}}\right) R_{in_1} + r_e i_{e_1} + r_e i_{e_2}$$

$$= i_{e_1}\left(\frac{R_{in_1}}{\beta_{ac}} + r_e\right) + r_e i_{e_2}$$

$$V_{in} = i_{e_1}(r_e) + r_e i_{e_2} \quad \text{——} ④ \qquad \left(\because r_e >> \frac{R_{in_1}}{\beta_{ac}}\right)$$

Apply crammers rule

$$i_{e_1} = \frac{\begin{vmatrix} V_{in} & -R_E \\ V_{in} & r_e \end{vmatrix}}{\begin{vmatrix} r_e + R_E & -R_E \\ r_e & r_e \end{vmatrix}} = \frac{V_{in} r_e + R_E V_{in}}{(r_e + R_E) r_e + R_E r_e}$$

$$= \frac{(r_e + R_E) V_{in}}{r_e [r_e + R_E + R_E)}$$

$$= \frac{(r_e + R_E) V_{in}}{r_e (r_e + 2R_E)} \quad \text{——} ⑤$$

and

$$i_{e_2} = \frac{\begin{vmatrix} r_e + R_E & V_{in} \\ r_e & V_{in} \end{vmatrix}}{\begin{vmatrix} r_e + R_E & -R_E \\ r_e & r_e \end{vmatrix}} = \frac{(r_e + R_E) V_{in} - V_{in} r_e}{(r_e + R_E) r_e + R_E r_e}$$

$$= \frac{r_e V_{in} + R_E V_{in} - V_{in} r_e}{r_e [r_e + R_E + R_E]}$$

$$= \frac{R_E V_{in}}{r_e (r_e + 2R_E)}$$

The output voltage $V_o = V_{c_2} - V_{c_1}$

$$= R_c i_{c_2} - (-R_c i_{c_1})$$

$$= R_c i_{c_2} + R_c i_{c_1} \Rightarrow R_c (i_{c_1} + i_{c_2})$$

$$\Rightarrow R_c (i_{e_1} + i_{e_2}) \quad (\because i_c \approx i_e)$$

$$V_o = R_c \left[\frac{(r_e + R_E) V_{in}}{r_e (r_e + 2R_E)} + \frac{R_E V_{in}}{r_e (r_e + 2R_E)} \right]$$

$$= R_c \left[\frac{(r_e + R_E) V_{in} + R_E V_{in}}{r_e (r_e + 2R_E)} \right]$$

$$= R_c \left[\frac{(r_e + R_E + R_E) V_{in}}{r_e (r_e + 2R_E)} \right] \Rightarrow R_c \left[\frac{(r_e + 2R_E) V_{in}}{r_e (r_e + 2R_E)} \right]$$

$$V_o = \frac{R_c}{r_e} \cdot V_{in}$$

$$\Rightarrow \frac{V_o}{V_{in}} = \frac{R_c}{r_e} \Rightarrow \boxed{A_d = \frac{R_c}{r_e}}$$

ii) Input resistance :-

$$R_i = \frac{V_{in_1}}{I_{b_1}}$$

w.k.T $I_{b_1} = \frac{ie_1}{\beta_{ac}}$

$$\Rightarrow R_i = \frac{V_{in_1}}{ie_1/\beta_{ac}} \Rightarrow \frac{V_{in_1}\,\beta_{ac}}{ie_1}$$

w.k.T $ie_1 = \frac{(r_e + R_E)\,V_{in}}{r_e\,(r_e + 2R_E)}$

$$\Rightarrow R_i = \frac{\frac{V_{in_1}\,\beta_{ac}}{(r_e+R_E)\,V_{in}}}{r_e\,(r_e+2R_E)} = \frac{\beta_{ac}\,r_e\,(r_e+2R_E)}{r_e+R_E}$$

consider $R_E >> r_e$

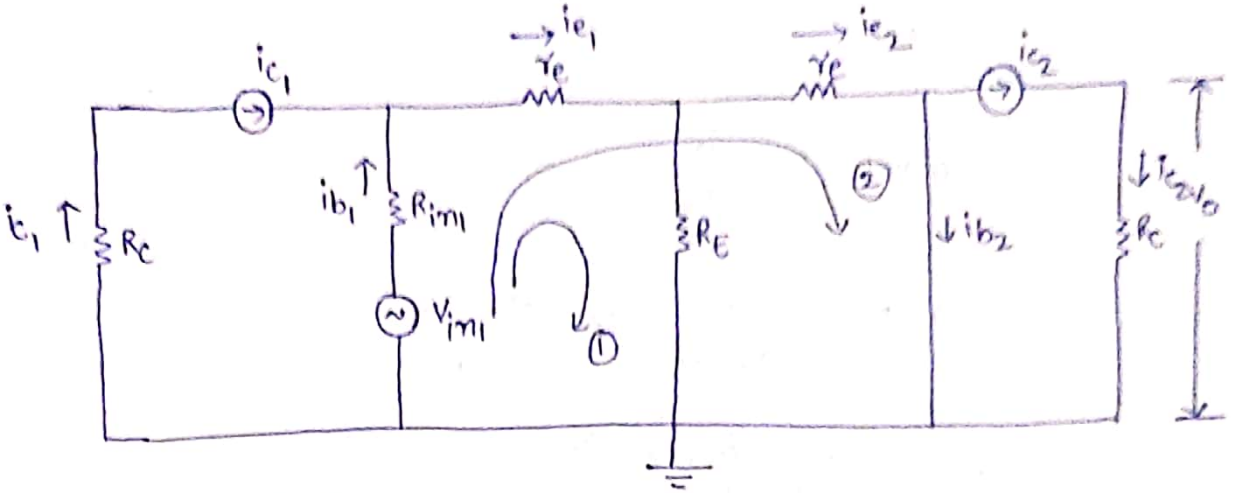
$$\Rightarrow R_i = \frac{\beta_{ac}\,r_e\,(2R_E)}{R_E}$$

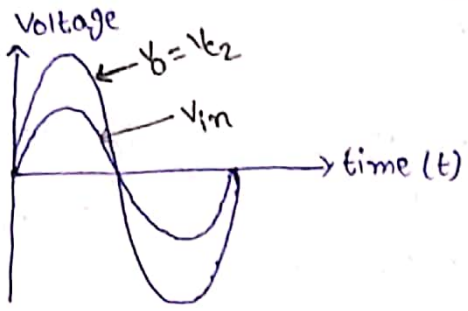
$$\Rightarrow \boxed{R_i = 2\beta_{ac}\,r_e}$$

iii) output resistance :- In this configuration, the output is taken between 2 collector terminals so,

$$\boxed{R_{o1} = R_{o2} = R_C} \quad (or)\ R_{c_1} = R_{c_2} = R_C$$

4. Single Input unbalanced output differential Amplifier :-





i) Voltage gain (A_d) :-

output voltage $V_o = V_{c_2}$

$= R_c\, ic_2$

$= R_c\, ie_2 \quad (\because ic_2 \simeq ie_2)$

[∵ Procedure same as Single Input balanced output for calculating ie_2 value]

$$V_o = R_c \left[\frac{R_E V_{in}}{r_e(r_e + 2R_E)} \right]$$

$$= R_c \left\{ \frac{R_E V_{in}}{r_e(2R_E)} \right\} \quad \left[\because \text{If } R_E >> r_e,\ r_e + 2R_E \approx 2R_E \right]$$

$$V_o = R_c \left[\frac{V_{in}}{2r_e} \right]$$

$$\Rightarrow \frac{V_o}{V_{in}} = \frac{R_c}{2r_e} \Rightarrow \boxed{A_d = \frac{R_c}{2r_e}}$$

The voltage gain is half the gain of Single Input balanced output

ii) Input resistance :-

$$R_i = 2\beta_{ac} r_e$$

→ The procedure is same as single Input balanced output differential Amplifier I/p resistance

iii) output resistance (R_o) :-

In this configuration output is taken between only one collector terminal so,

$$R_{o_2} = R_C$$

comparisions of different configurations (using r-parameters)

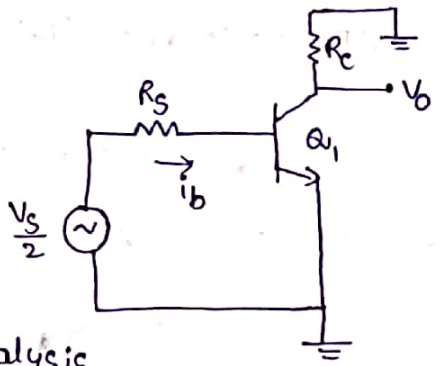
configuration	Differential gain (A_d)	Input resistance (R_i)	output resistance (R_o)
Dual Input balanced output	$A_d = \frac{R_C}{r_e}$	$R_{i_1} = R_{i_2} = 2\beta_{ac} r_e$	$R_{o_1} = R_{o_2} = R_C$
Dual Input unbalanced output	$A_d = \frac{R_C}{2r_e}$	$R_{i_1} = R_{i_2} = 2\beta_{ac} r_e$	$R_{o_2} = R_C$
Single Input balanced output	$A_d = \frac{R_C}{r_e}$	$R_i = R_{i_1} = 2\beta_{ac} r_e$	$R_{o_1} = R_{o_2} = R_C$
Single Input unbalanced output	$A_d = \frac{R_C}{2r_e}$	$R_i = R_{i_1} = 2\beta_{ac} r_e$	$R_{o_2} = R_C$

A.c Analysis of differential Amplifier using h-parameters

In differential Amplifier, 2 transistors has similar characteristics i.e Input voltage $V_{in1} = V_{in2} = V_{in}$ and $R_{E1} = R_{E2} = R_E$.

i) Differential Gain (A_d) :-

To caluclate differential gain, consider only one transistor. This is called as Half circuit concept Analysis.



The equivalent circuit diagram for above circuit can be shown in fig. below, neglecting h_{oe}.

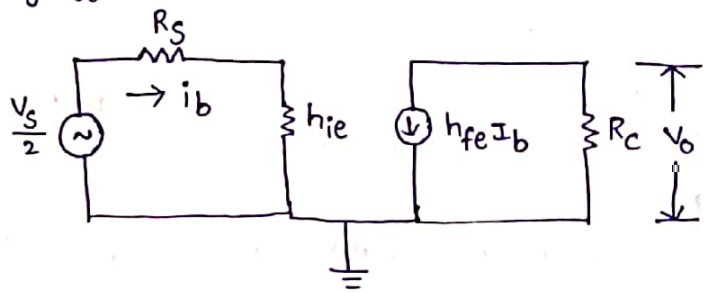


Fig:- Approximate hybrid model

Apply KVL to Input loop,

$$\frac{V_S}{2} = R_S i_b + h_{ie} i_b$$

$$= i_b (R_S + h_{ie})$$

$$\Rightarrow i_b = \frac{V_S}{2(R_S + h_{ie})} \quad \text{— (1)}$$

Apply KVL to output loop,

$$V_o = -h_{fe} I_b R_C \quad \text{— (2)}$$

substitute eq (1) in eq (2)

$$\Rightarrow V_o = -h_{fe} \left[\frac{V_S}{2(R_S + h_{ie})} \right] R_C$$

$$\Rightarrow \frac{V_o}{V_s} = \frac{-h_{fe} R_c}{2(R_s + h_{ie})}$$

'−' sign indicates the phase difference between Input and output.

magnitude of differential gain A_d is

$$\boxed{A_d = \frac{V_o}{V_s} = \frac{h_{fe} R_c}{2(R_s + h_{ie})}} \rightarrow \text{for Imbalanced output.} \quad -③$$

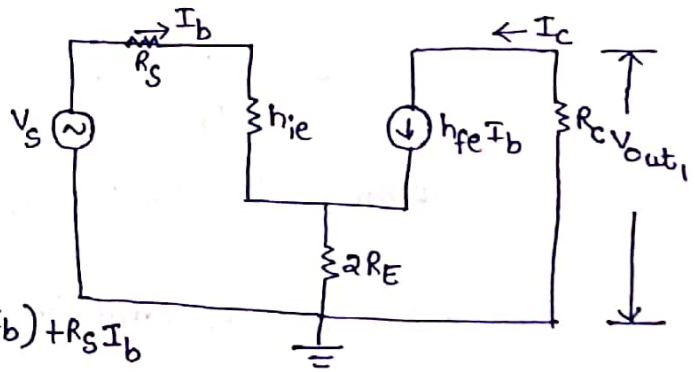
Note :- For Balanced output, $A_d = 2 \times \frac{h_{fe} R_c}{2(R_s + h_{ie})}$

$$\boxed{A_d = \frac{h_{fe} R_c}{R_s + h_{ie}}}$$

ii) common mode gain (A_c) :-

For common mode gain $V_c = \frac{V_1 + V_2}{2} = \frac{V_s + V_s}{2} = V_s$

The equivalent circuit as shown in figure,



Apply KVL to Input loop,

$$V_s = I_b h_{ie} + 2R_E (I_b + h_{fe} I_b) + R_s I_b$$

$$= I_b h_{ie} + 2R_E (1 + h_{fe}) I_b + R_s I_b$$

$$= \left(h_{ie} + (1 + h_{fe}) 2R_E + R_s\right) I_b \quad -④$$

At output, $V_o = -I_c R_c$

$$= -h_{fe} I_b R_c \quad -⑤$$

we know that, $V_o = A_c \cdot V_s \Rightarrow A_c = \frac{V_o}{V_s}$ —⑥

Substitute eq ④, ⑤ in eq ⑥

$$A_c = \frac{-h_{fe} I_b R_c}{(h_{ie} + (1+h_{fe}) 2R_E + R_s) I_b}$$

$$\Rightarrow \boxed{A_c = \frac{-h_{fe} R_c}{R_s h_{ie} + (1+h_{fe}) 2R_E}} \quad -⑦$$

iii) CMRR:- $\quad CMRR = \left| \frac{A_d}{A_c} \right|$

$$= \frac{h_{fe} R_c}{2(R_s + h_{ie})} \times \frac{R_s + h_{ie} + (1+h_{fe}) 2R_E}{h_{fe} R_c}$$

$$\boxed{CMRR = \frac{R_s + h_{ie} + 2R_E (1+h_{fe})}{2(R_s + h_{ie})}} \quad -⑧$$

iv) Input Impedance (or) Input resistance (R_i) :-

$$R_i = \frac{V_s}{I_b} \quad -⑨$$

from eq ①, $I_b = \frac{V_s}{2(R_s + h_{ie})}$

substitute I_b value in eq ⑨,

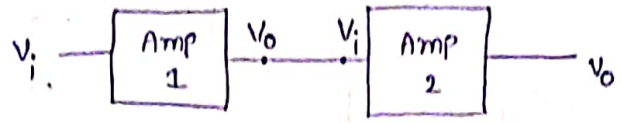
$$R_i = \frac{V_s}{V_s / 2(R_s + h_{ie})} \Rightarrow \boxed{R_i = 2(R_s + h_{ie})}$$

v) Output resistance (R_o) :- output taken between one of the output terminal.

i.e $\boxed{R_o = R_c}$

D.C coupling:-

The first stage output is connected to the next stage Input is called coupling.



It is also called as cascading (or) multistageing (or) Direct coupling.

cascaded differential Amplifier stages :- (or) Intermediate stage of an OP-Amp

The main purpose of the cascaded differential Amplifier is to provide high gain to the differential mode signal and cancel the common mode signal.

→ In cascading of differential Amplifiers, output of one stage given to Input of next stage.

→ In this circuit, two differential Amplifiers are connected in series.

The series connection of differential Amplifiers is called cascading of differential Amplifiers, which is used to produce single ended output.

The circuit diagram for cascaded differential Amplifier is shown in fig. below

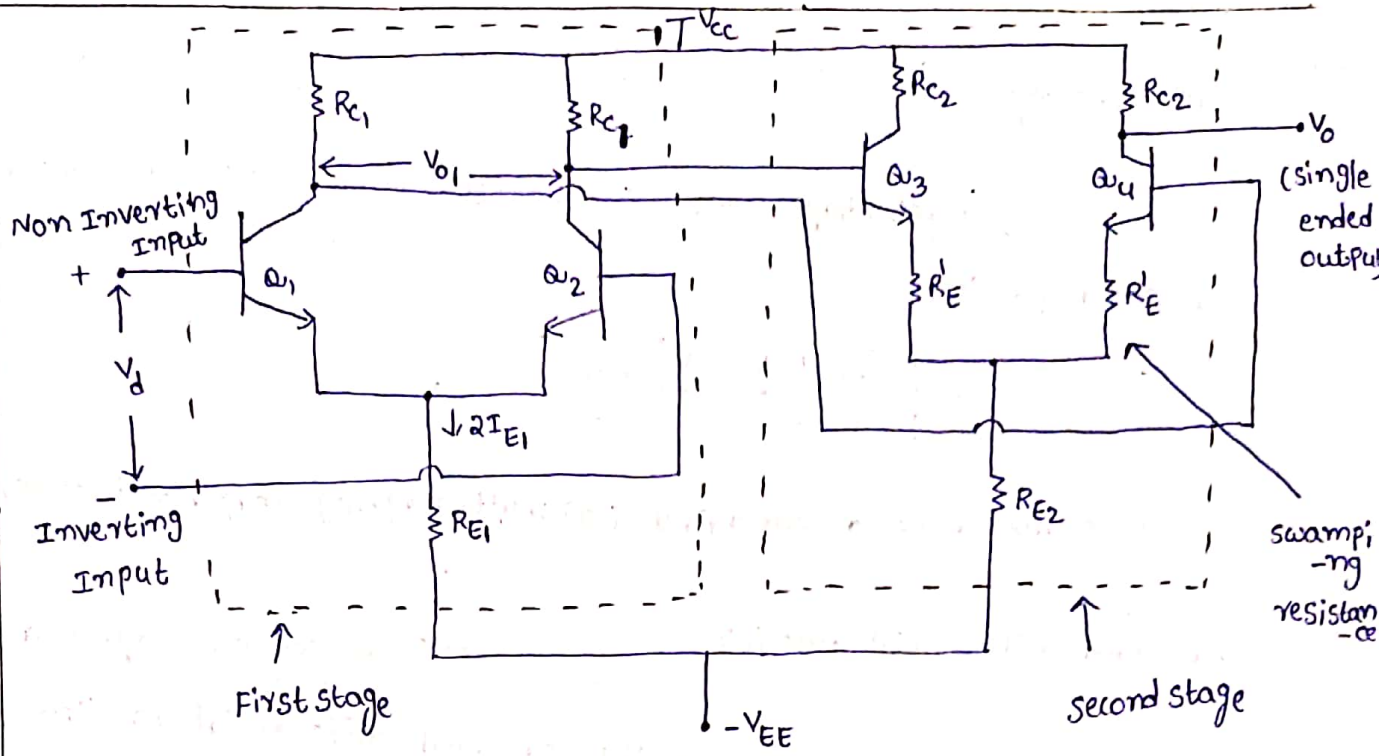


Fig:- cascaded differential Amplifier stages.

From figure,

Q_1, Q_2 are first stage transistors i.e dual Input balanced output configuration. Q_3, Q_4 are second stage transistors i.e dual Input unbalanced output configuration.

→ The collector resistances of 1st stage are equal i.e R_{C_1} while collector resistances of 2nd stage are equal R_{C_2}.

→ First stage is a dual Input balanced output differential Amplifier . it uses emitter resistance R_{E_1} which carries a current $2I_{E_1}$, where I_{E_1} is the emitter current of transistor Q_1 which is same as emitter current of transistor Q_2 as the transistors are perfectly matched.

→ The second stage uses a pair of swamping resistances and emitter resistance R_{E2}. It carries a current of $2I_{B3}$ $2I_{E3}$.

Swamping resistances :-

To achieve high Input resistance, external resistances R'_E are connected in series with each emitter of transistor. Such resistances are called swamping resistors.

The various effects of swamping resistances used in differential Amplifiers are,

i) Increase Input resistance

ii) minimization of changes in transistor parameters due to change in temperature

iii) Increase in the linearity range of differential Amplifier.

iv) Reduction in ~~differential~~ common mode gain.

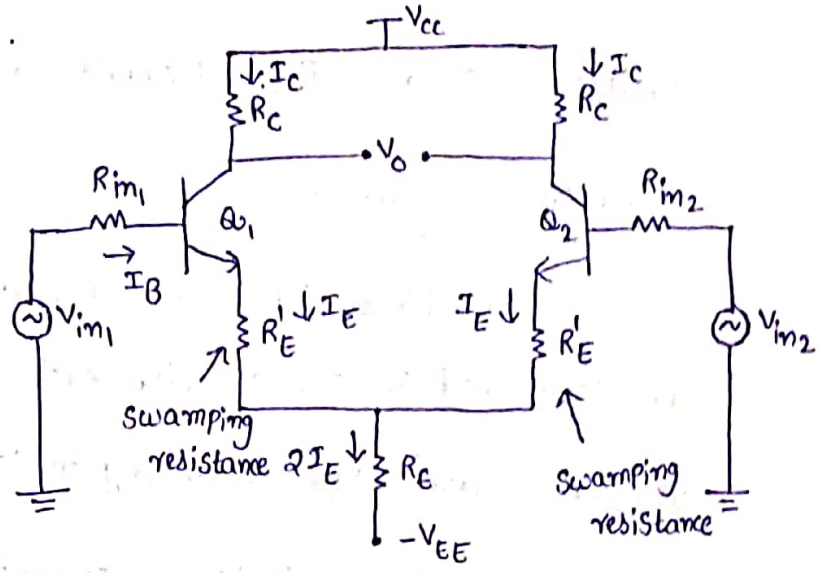
→ The main advantages of cascaded differential Amplifiers are

i) Gain value Increases

ii) Input Impedance is very high

iii) CMRR Increases.

Differential Amplifier with Swamping resistors (Extra syllabus)



D.c Analysis

For calculating D.c Analysis, consider V_{in_1}, V_{in_2} values should be zero.

Apply KVL at Input loop,

$$-I_B R_{in_1} - V_{BE} - I_E R'_E - 2I_E R_E + V_{EE} = 0 \quad \text{—①}$$

w.k.t $\quad I_B = \frac{I_E}{\beta_{dc}} \quad \text{—②}$

substitute eq② in ①

$$-\frac{I_E}{\beta_{dc}} R_{in_1} - I_E R'_E - 2I_E R_E - V_{BE} + V_{EE} = 0$$

$$V_{EE} - V_{BE} = I_E \left(-\frac{R_{in_1}}{\beta_{dc}} + R'_E + 2R_E \right)$$

$$\Rightarrow \boxed{I_E = \frac{V_{EE} - V_{BE}}{2R_E + R'_E}} \qquad \left[\because R'_E + 2R_E >> \frac{R_{in}}{\beta_{dc}} \right)$$

Apply KVL to output loop,

$$\boxed{V_{CE} = V_{CC} + V_{BE} - I_C R_C}$$

A.c Analysis:-

For calculating A.c Analysis, D.c voltages i.e V_{cc} and $-V_{EE}$ should be zero.

i) Differential gain $(A_d) = \dfrac{h_{fe} R_C}{R_S + h_{ie} + (1+h_{fe}) R'_E}$ → Dual Input Balanced output

and $A_d = \dfrac{h_{fe} R_C}{2[R_S + h_{ie} + (1+h_{fe}) R'_E]}$ → Dual Input unbalanced output

ii) common mode gain for both transistors is

$$A_c = \frac{h_{fe} R_C}{R_S + h_{ie} + (1+h_{fe})(R'_E + 2R_E)}$$

iii) Input Impedance, $R_{in} = 2[R_S + h_{ie} + (1+h_{fe}) R'_E]$

iv) output Impedance, $R_o = R_C$

Methods of Improving CMRR :-

$$CMRR = \left| \frac{A_d}{A_c} \right|$$

To Improve the CMRR, common mode gain A_c must be reduced.

→ In differential Amplifier circuit, R_E can be replaced by 2 methods

i) constant current bias method

ii) use of current mirror circuit

i) constant current bias method :-

In the differential Amplifier circuit, the resistance R_E can be replaced by constant current source method gives effect of a very high resistance with out affecting Q-Point values of differential Amplifier.

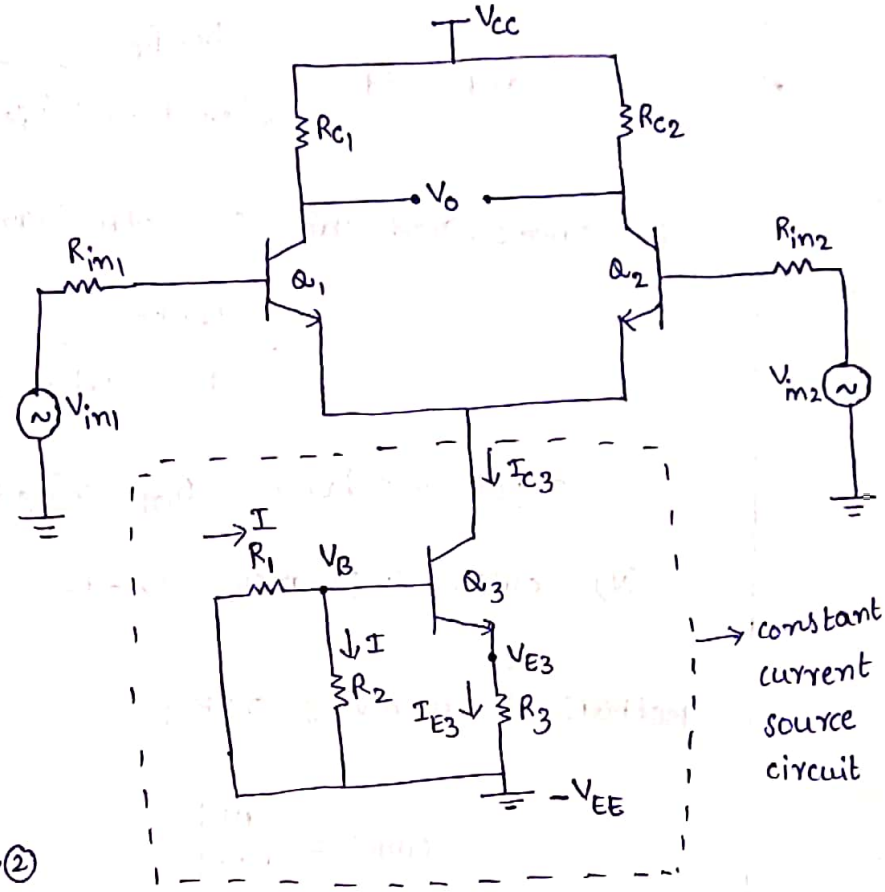


Fig:- constant current source

Apply KVL to Q_3

$$-IR_1 - IR_2 - (-V_{EE}) = 0$$

$$-I(R_1+R_2) = -V_{EE}$$

$$\Rightarrow I = \frac{V_{EE}}{R_1+R_2} \quad \text{— ①}$$

consider

$$V_B = -IR_1 \quad \text{— ②}$$

Substitute eq① in eq②

$$V_B = \left(\frac{-V_{EE}}{R_1+R_2}\right) R_1 \quad \text{— ③}$$

w.k.t $V_{BE} = V_B - V_E$

$$\Rightarrow V_E = V_B - V_{BE} \quad \text{— ④}$$

Substitute eq③ in ④

$$V_E = \left(\frac{-V_{EE}}{R_1+R_2}\right) R_1 - V_{BE} \quad \text{— ⑤}$$

From figure,

$$I_{E3} = \frac{V_E - (-V_{EE})}{R_3} = \frac{V_E + V_{EE}}{R_3} \quad \text{—⑥}$$

Sub. eq⑤ in eq⑥

$$I_{E3} = \frac{V_B - V_{BE} + V_{EE}}{R_3} = \frac{\frac{-V_{EE} R_1}{R_1 + R_2} - V_{BE} + V_{EE}}{R_3}$$

$$= \frac{-V_{EE} R_1 - V_{BE}(R_1 + R_2) + V_{EE}(R_1 + R_2)}{(R_1 + R_2) R_3}$$

$$= \frac{-V_{EE} R_1 - V_{BE} R_1 - V_{BE} R_2 + V_{EE} R_1 + V_{EE} R_2}{(R_1 + R_2) R_3}$$

$$= \frac{-V_{BE}(R_1 + R_2) + V_{EE} R_2}{(R_1 + R_2) R_3}$$

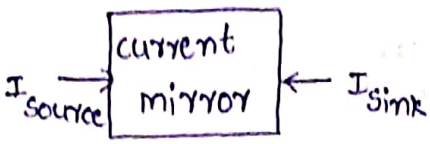
$$\boxed{I_{E3} = I_{C3} = \frac{V_{EE}\left(\frac{R_2}{R_1 + R_2}\right) - V_{BE}}{R_3}} \quad \text{—⑦} \quad (\because I_{E3} \simeq I_{C3})$$

Thus, V_{EE}, R_1, R_2, R_3 are constants, current I_{C3} almost equal to I_{E3} also constant. So, transistor Q_3 act as constant current source.

ii) current mirror circuit :-

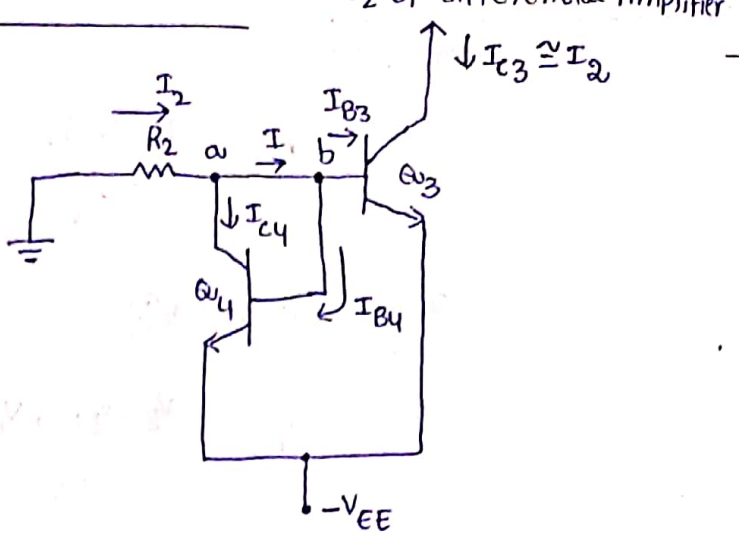
The circuit in which the output current is forced to equal the Input current is called as "current mirror circuit".

→ In a current mirror circuit, the output current is the mirror Image of Input current.



$I_{source} = I_{sink}$

a) Block diagram



b) circuit diagram

The circuit consists of two matched transistors Q_3, Q_4.

i.e $V_{BE3} = V_{BE4}$

$I_{B3} = I_{B4}$

and $I_{C3} = I_{C4}$

Apply KCL at node 'A'

$$I_2 = I_{C4} + I \quad \text{——} (8)$$

Apply KCL at node 'B'

$$I = I_{B3} + I_{B4}$$

$$= 2I_{B3} = 2I_{B4} \quad \text{——} (9) \qquad (\because I_{B3} = I_{B4})$$

From eq (8), $I_2 = I + I_{C4}$

$$= 2I_{B4} + I_{C4} \quad (\text{or}) \quad 2I_{B3} + I_{C3} \quad \text{——} (10)$$

W.K.T $I_B = \frac{I_C}{\beta}$

So eq (10) becomes, $I_2 = 2\left(\frac{I_{C4}}{\beta}\right) + I_{C4}$

$$I_2 = 2\left(\frac{I_{C3}}{\beta}\right) + I_{C3}$$

consider $\frac{I_{C3}}{\beta}$ is very small value,

$$\Rightarrow \boxed{I_2 = I_{C3}}$$

It indicates output current is equal to mirror current of Input.

Apply KVL at transistor Q_3,

$$-I_2R_2 - V_{BE3} - (-V_{EE}) = 0$$

$$V_{EE} - V_{BE3} = I_2R_2$$

$$\Rightarrow \boxed{I_2 = \frac{V_{EE} - V_{BE3}}{R_2}}$$

Level Translator :- (or) Level shift stage in OP-Amp :-

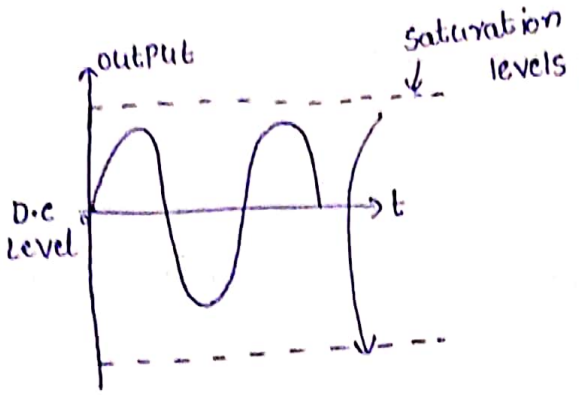
As the coupling capacitors are not used to couple the Amplifiers in the cascaded stage, D.c biasing voltage level propagates through the Amplifier chain. This finally appears as a significant d.c component at the output along with a.c output.

In presence of d.c component at output, there are some effects

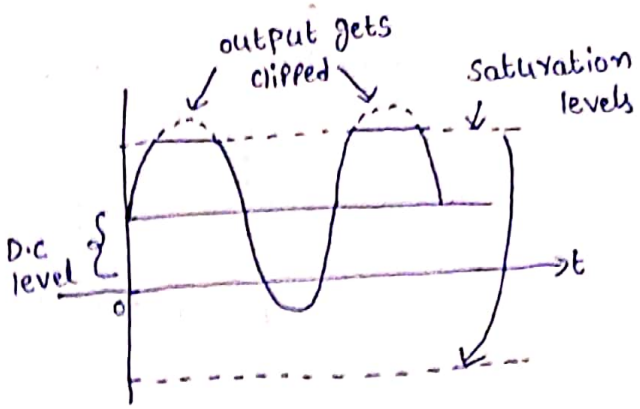
i) The output gets distorted.

ii) It limits the maximum output voltage swing.

The main purpose of the level shifting is to shift the output d.c level towards the ground, with minimum change in A.c signal.

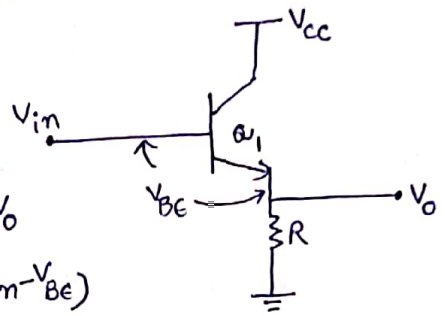


a) output with zero D.C level



b) Distorted output due to additional D.C level

circuit 1 :- Simplest level shifting Network (Emitter follower)



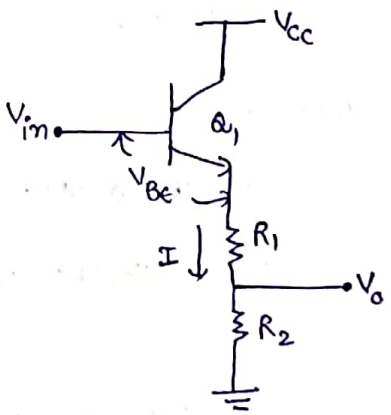
Apply KVL

$$V_o = V_{in} - V_{BE} \quad (\because V_{in} = V_{BE} + V_o \Rightarrow V_o = V_{in} - V_{BE}) \quad \text{—①}$$

In the circuit,
The amount of shift obtained is equal to V_{BE} which is almost 0.7V.

circuit 2 :- (common collector stage)

In Previous circuit, shift is 0.7V is not sufficient. hence the circuit is modified with help of 2 resistances R_1 and R_2.



It is a common collector stage, which also act as buffer to Isolate high gain stages from output stage.

Apply KVL to Base-emitter Loop

$$V_{in} - V_{BE} - IR_1 - IR_2 = 0 \Rightarrow V_{in} - V_{BE} = I(R_1 + R_2)$$

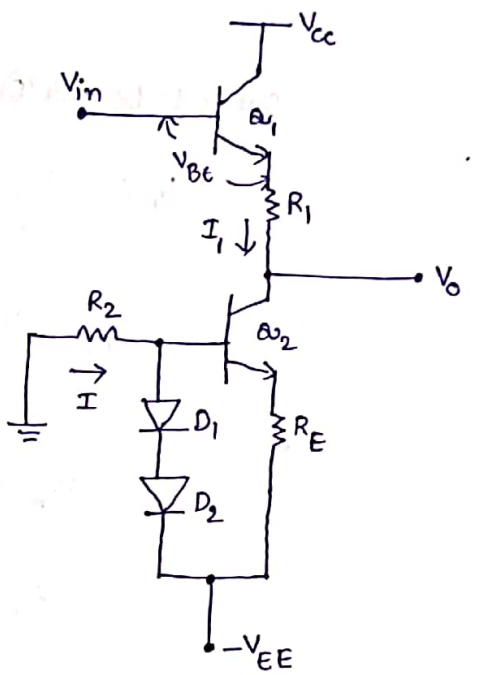
$$\boxed{I = \frac{V_{in} - V_{BE}}{R_1 + R_2}} \quad -(2)$$

and $V_o = IR_2 \Rightarrow V_o = \left(\frac{V_{in} - V_{BE}}{R_1 + R_2}\right) R_2$

→ The main draw back of this circuit is that signal voltage also attenuated by the factor $\frac{R_2}{R_1 + R_2}$.

circuit3 :- (constant current source)

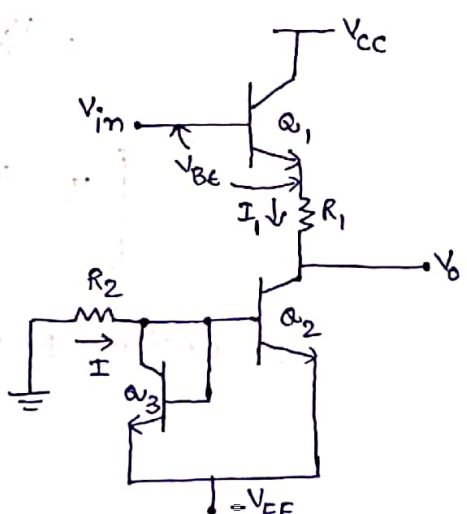
In the above circuit, resistor R_2 can be replaced by constant current source.



From the circuit,

$$\boxed{V_o = V_{in} - V_{BE} - I_1 R_1} \quad -(3)$$

circuit 4 :- (current mirror circuit)



In current mirror circuit,

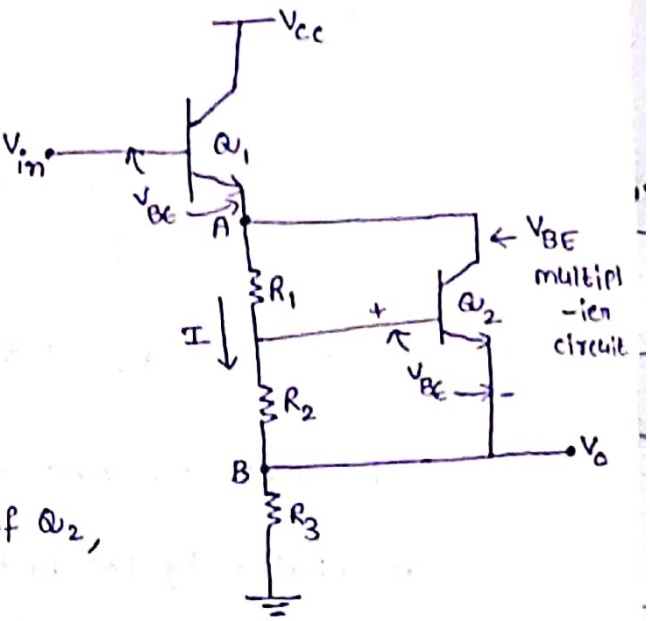
$$I_1 = I$$

and. $I_1 = I = \frac{V_{EE} - V_{BE}}{R_2}$

and $\boxed{V_o = V_{in} - V_{BE} - I_1 R_1}$ $-(4)$

By choosing proper values of I, R_1 the output V_o can be zero level.

circuit 5 (multiplier circuit)



It is another level shifting network with V_{BE} multiplier circuit.

From figure,

$$V_{AB} = I(R_1+R_2) \quad \text{—⑤}$$

Apply KVL to Base emitter loop of Q_2,

$$V_{BE} = IR_2 \Rightarrow I = \frac{V_{BE}}{R_2} \quad \text{—⑥}$$

substitute eq⑥ in eq⑤

$$V_{AB} = \frac{V_{BE}}{R_2}(R_1+R_2)$$

$$V_{AB} = V_{BE}\left(\frac{R_1}{R_2}+1\right) \quad \text{—⑦}$$

and

$$V_o = V_{in} - V_{AB} - V_{BE}$$

$$= V_{in} - V_{BE} - \left[V_{BE}\left(\frac{R_1}{R_2}+1\right)\right]$$

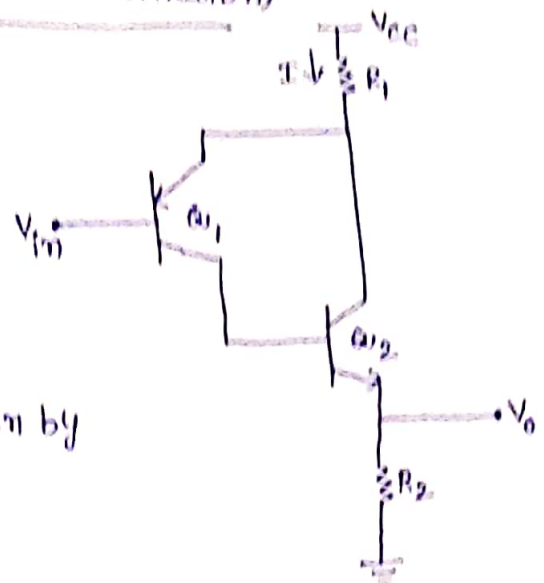
$$= V_{in} - V_{BE}\left[1+\frac{R_1}{R_2}+1\right]$$

$$\boxed{V_o = V_{in} - V_{BE}\left[2+\frac{R_1}{R_2}\right]}$$

By selecting proper values of R_1, R_2 to adjust V_o to zero.

circuit 6 (PNP and NPN transistor combination)

In this level shifting network can be used for PNP and NPN transistors.



The output voltage V_o is given by

$$V_o = \frac{R_2}{R_1}(V_{cc} - V_{BE} - V_{in})$$

G. Venkata Hanuman
Asst. Prof
ECE

2. Operational Amplifiers

An operational Amplifier is a direct coupled high-gain Amplifier usually consisting of one (or) more differential Amplifiers and usually followed by a level translator and output stage.

→ Operational Amplifiers mainly 2 types

i) open loop OP-Amps

ii) closed loop OP-Amps

i) open loop OP-Amps :-

There is no feed back present, gain of the amplifier is high.

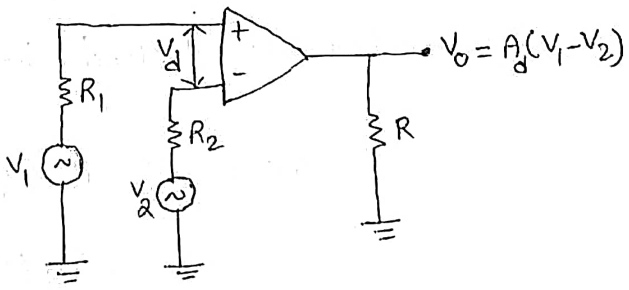
There are 3 open loop configurations

i) differential Amplifier

ii) Inverting Amplifier

iii) Non-Inverting Amplifier.

i) differential Amplifier :-



'+' → Non-Inverting terminal

'−' → Inverting terminal

From the figure,

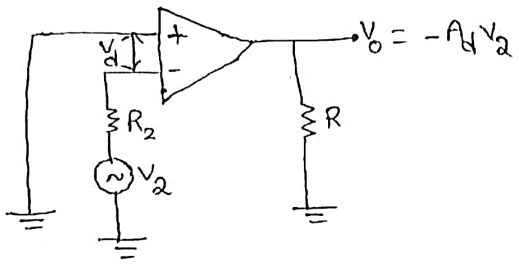
Input voltage V_1 is applied to Non-Inverting terminal through the resistor R_1.

V_2 is connected to Inverting terminal through the resistor R_2

differential voltage gain $V_d = V_1 - V_2$

output voltage, $V_0 = A_d (V_1 - V_2)$

ii) Inverting Amplifier :-

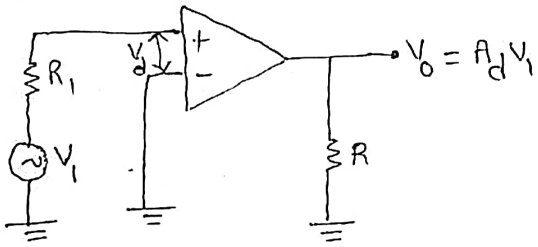


In this configuration, Input is applied to Inverting terminal & Non Inverting terminal is connected to ground i.e $V_1 = 0$

w.k.T $V_0 = A_d (V_1 - V_2)$

$= A_d (0 - V_2)$ $\Rightarrow \boxed{V_0 = -A_d V_2}$

iii) Non-Inverting Amplifier :-



In this configuration, Input is applied to Non-Inverting terminal & Inverting terminal is connected to ground i.e $V_2 = 0$

w.k.T $V_0 = A_d (V_1 - V_2)$

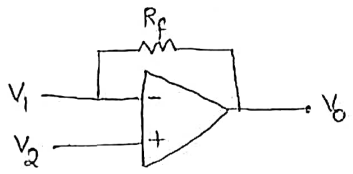
$= A_d (V_1 - 0)$

$\boxed{V_0 = A_d V_1}$

2. closed Loop OP-Amp :-

In closed Loop operation, the output is connected to Input is called feed back.

Generally -Ve feed back is used.



In this fig,

some part of the output is given to Input, through the resistor is called feed back resistor.

Advantages

→ It stabilizes the gain

→ Band width Increases

→ Input and output resistances are changed

→ Decreases Non-linear distortion.

Characteristics of operational Amplifiers :-

operational Amplifiers mainly 2types

1. Ideal OP-Amp
2. Practical OP-Amp

1. Ideal OP-Amp characteristics :-

1. Infinite Input resistance
2. zero output resistance
3. Infinite Voltage gain

4. zero offset voltage
5. Infinite Band width
6. Infinite CMRR
7. Infinite Slew rate
8. No effect to temperature

1. Infinite Input resistance ($R_i = \infty$) :-

The Input resistance is measured at either Inverting (or) Non-Inverting terminal with other terminal is grounded. In Ideal OP-Amp the current at Inverting and Non-Inverting terminal is zero. There is no loading on preceding stage.

2. zero output resistance ($R_o = 0$) :-

The output resistance is measured between output terminal and ground. Since $R_o = 0$, output of OP-Amp does not depend on current flows through it. Therefore, output can drive other devices.

3. Infinite voltage gain ($A_{OL} = \infty$) :-

It is defined as the ratio of output voltage to the difference Input voltage. For, Ideal OP-Amp the voltage gain is Infinity.

4. zero offset voltage ($V_{ios}=0$) :-

For an Ideal OP-Amp, Input is zero ($V_1=V_2=0$), The output voltage also zero.

The presence of small output voltage through $V_1=V_2=0$ is called "offset".

5. Infinite Band width ($B\omega=\infty$) :-

Band width is nothing but difference between upper cut-off frequency and lower cut-off frequency.

The operating frequency range from 0 to ∞, so $B.\omega=\infty$.

6. Infinite CMRR ($CMRR=\infty$) :-

CMRR is defined as the ratio of differential gain (A_d) to common mode gain (A_c).

$$CMRR = \frac{A_d}{A_c}$$

For Ideal OP-Amp, $A_c=0$ $\Rightarrow CMRR = \frac{A_d}{0}$ $\Rightarrow \boxed{CMRR=\infty}$

7. Infinite Slew rate ($S=\infty$) :-

Slew rate is defined as the "maximum rate of change of output voltage for each unit time".

$$S = \left.\frac{dV_o}{dt}\right|_{max}$$

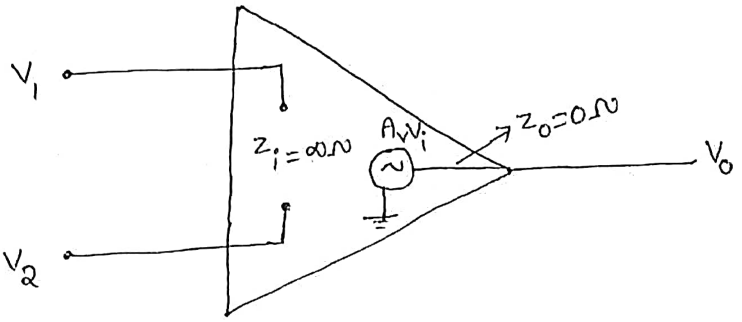
→ Slew rate expressed in V/μS

→ For Ideal OP-Amp, Slew rate is Infinite

8. No Effect to temperature :-

The characteristics of OP-Amp donot change with temperature.

The equivalent circuit of Ideal OP-Amp is shown in fig.

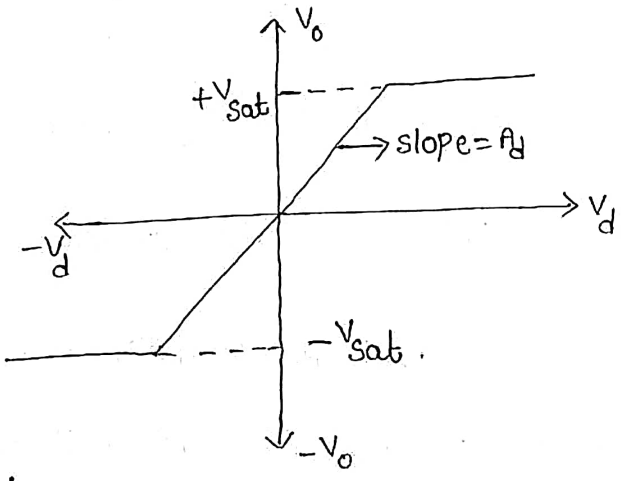


Ideal voltage transfer curve :-

we know that, the output voltage is $V_o = A_d V_d$

$= A_d (V_1 - V_2)$

The graph is drawn between output voltage V_o, Input voltage V_i keeping A_d is constant.



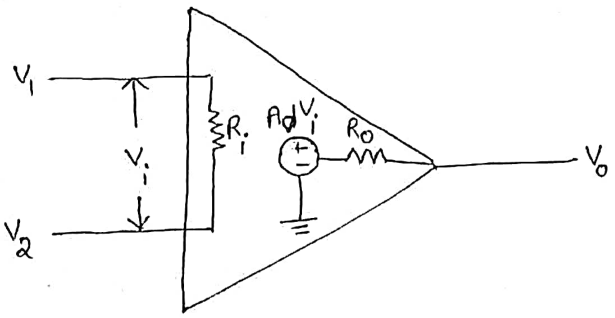
From the graph, output voltage cannot exceed the +ve and -ve saturation voltages.

because, the output voltage is directly proportional to difference of Input voltages. So, output voltages reaches to saturation voltages, the output voltage remains constant.

The curve is called Ideal voltage transfer curve.

2. Practical OP-Amp :-

The equivalent circuit is shown in fig.



The output voltage $V_o = A_d (V_1 - V_2)$

Practical, OP-Amp characteristics

i) Input resistance (R_i) is 2mΩ

ii) output resistance (R_o) is 75Ω

iii) open loop voltage gain (A_{OL}) is 2×10^5

iv) Bandwidth is 1MHz

v) CMRR is 90dB

vi) slew rate is 0.5 V/μsec

Types of Integrated circuits :-

There are 2 types

1. Analog Integrated circuits
2. Digital Integrated circuits

1. Analog Integrated circuits :-

Integrated circuits that operate over an entire range of continuous values of signal Amplitude are called Analog Integrated circuits.

These are further classified into 2types

1. Linear Integrated circuits
2. Radio frequency Integrated circuits

i) Linear Integrated circuits:-

An Analog Ic is said to be linear, if there exists a Linear relation between its voltage and current.

Ex:- IC741, 8-Pin Dual-In-Line package (DIP).

ii) Radio frequency Integrated circuits:-

An analog Ic is said to be Non linear, if there exists a Non-linear relation between voltage and current.

2. Digital Integrated circuits:-

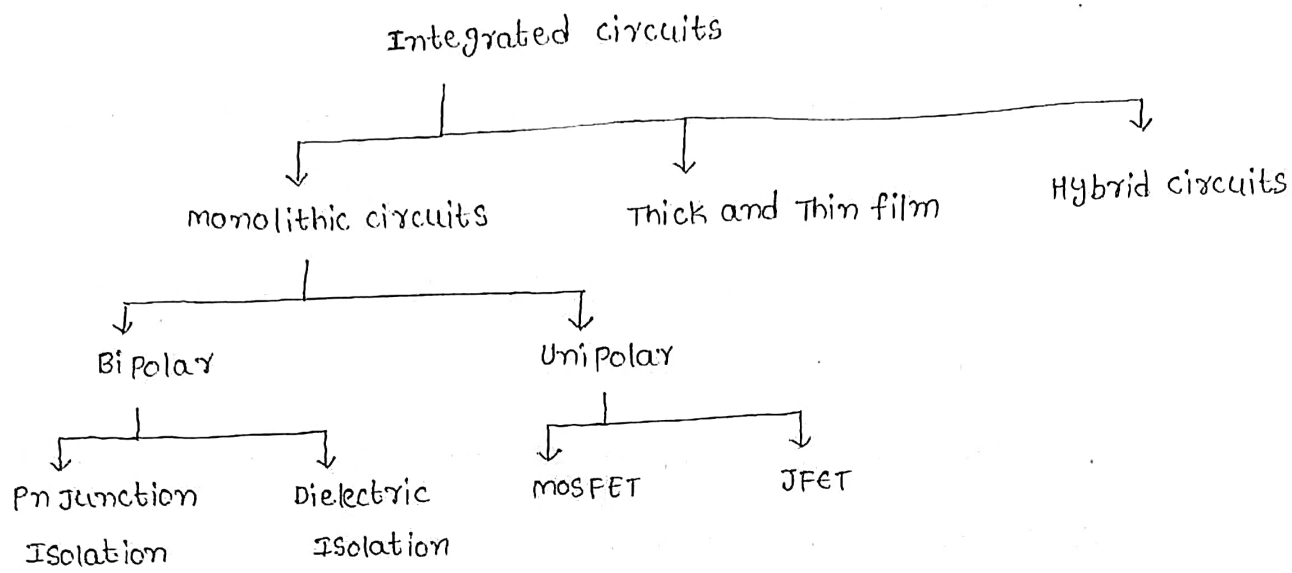
If the Integrated circuits operates only at a few pre-defined levels Instead of operating for an entire range of continuous values of signal Amplitude, then these are called Digital Integrated circuits.

Ex:- Logic gates, multiplexers, shift registers Etc...

classifications of Operational Amplifiers:-

Classifications of Ic's :-

1) Based on fabrication :-



i) monolithic Ic's :-

All the circuit components, both Active and passive elements are connected in a single chip of silicon.

→ The word 'monolithic' is originated from Greek word means 'single stone' (or) 'one stone'.

→ mainly used monolithic Ic's because i) Lower cost
ii) High reliability

→ Based on active devices used, monolithic Ic's again classified into Bipolar and unipolar Ics.

Bipolar Ic's uses BJT's and unipolar Ic's use FET.

→ Depending upon Isolation technique, Bipolar Ic's divided into p-n Junction Isolation Ics and Dielectric Isolation Ic's.

2. Based on chip size and Levels of Integration :-

chip developement	chip size	Invented Year	uses
1. Small Scale Integration (SSI)	<100 active devices	1960	Integrated resistors, diodes, BJT's.
2. medium Scale Integration (MSI)	100 - 1000 active devices	1965-1970	BJT's and Enhanced MOSFETS
3. Large Scale Integration (LSI)	1000 - 10,000 active devices	1970-1975	MOSFETS
4. Very Large Scale Integration (VLSI)	>100000 active devices	1975	8-bit, 16-bit micro processors
5. Ultra Large Scale Integration (ULSI)	over 1 million active devices	-	Pentium microprocessors

3. Based on Signal Processed :-

It can be 4 types

1. Digital Integrated circuits
2. Analog Integrated circuits
3. mixed- signal Integrated circuits
4. memory- Integrated circuits

1. Digital Integrated circuits :-

They perform mathematical caluclations, flow of data and make decisions based on Boolean Logic Principles (either Logic '0' (or) Logic '1')

2. Based on chip size and Levels of Integration :-

chip developement	chip size	Invented Year	uses
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3. Based on signal Processed :-

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2. Analog Integrated circuits
3. mixed- signal Integrated circuits
4. memory- Integrated circuits

1. Digital Integrated circuits :-

They perform mathematical caluclations, flow of data and make decisions based on Boolean Logic Principles (either Logic '0' (or) Logic '1')

→ Digital Integrated circuits mainly used in computers, cell phones, Televisions.

→ It Includes microprocessors, micro controllers, logic circuits.

2. Analog Integrated circuits:-

Analog Integrated circuits amplify, filter and modify electrical signals.

For Ex, In cellular phones, they amplify and filter the Incoming signal from the phones antenna. The sound encoded into that signal has a low Amplitude level; after the circuit filters the sound signal from Incoming signal, the circuit Amplify sound signal and sends it to speaker in your cell phone, allowing you hear the voice on other end.

3. mixed signal circuits:-

In this type, to convert Analog signals to digital signals.

→ They convert analog voltage levels to digital number representation of voltage levels.

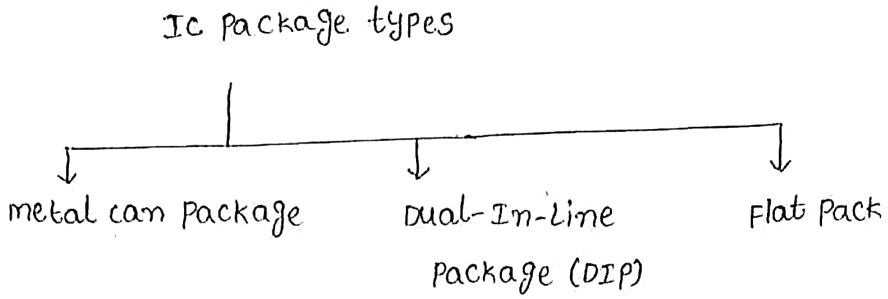
4. memory Integrated circuits:-

memory circuits perform caluclations and to save the data (or) Information.

→ Data it access → pictures, sound, text....

→ computer system may Include 20 to 40 memory chips.

Ic Package types :-



i) metal can Package :-

→ The metal sealing plate is at the bottom over which the chip is bonded.

→ The plane is effective for heat dissipation, hence this type used for power Amplifiers.

→ It also permits the External heat sink.

→ It also called as "Transistor Pack"

→ The available Pins are 3,5, 8, 10,12 Pins.

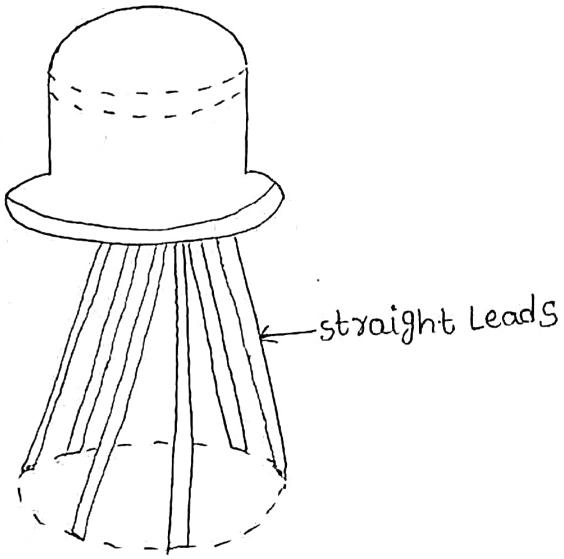


Fig :- To-5 style Package (6, 8, 10, 12 Lead)

ii) Dual-In-Line Package (DIP) :-

In this type, the chip is mounted Inside a Plastic (or) ceramic case.

→ It is easy to handle and most widely used.

→ The 8-Pin DIP is called mini DIP.

→ Available Pins are 12, 14, 16, 20.

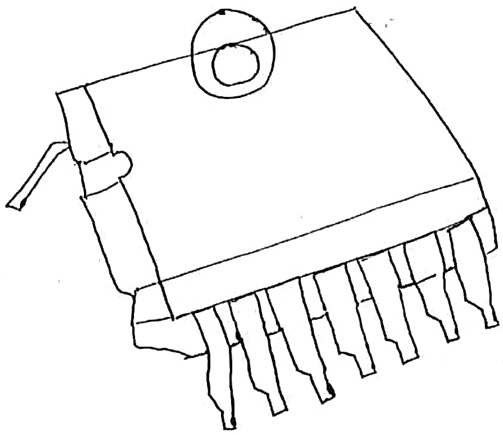


Fig:- 14, 16, Lead version of DIP.

iii) Flat Pack:-

In this type the chip is enclosed in a rectangular ceramic case.

→ The terminals are taken out through the sides and ends.

→ The available Pins are 8, 10, 14, 16 leads.

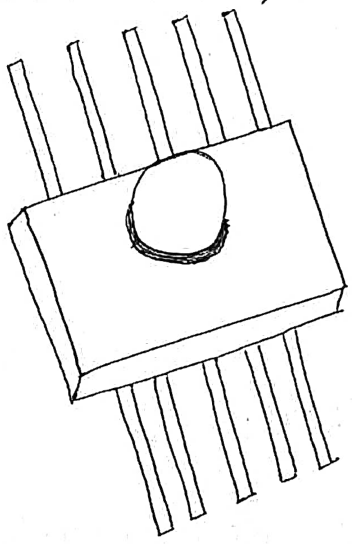


Fig:- 10-Lead Version of Flat Package

Selection of Ic Package :-

Type	criteria
1. metal can Package	i) Heat dissipation is Important ii) Applications FOR high Power Amplifers, Voltage regulators etc..
2. Dual InLine Package (DIP)	i) FOR Experimental (or) bread boarding purposes ii) If bending (or) soldering of the leads is not required. iii) suitable for printed circuit boards.
3. Flat Pack	i) more reliability is required ii) Light in weight iii) suitable for airbone Applications.

Power supply :-

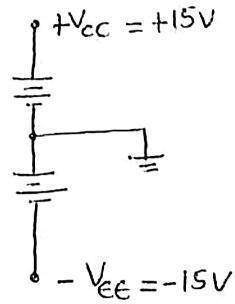
The op-Amp works on a dual supply. A dual supply consists of 2 supply voltages, they are +ve supply $+V_{cc}$ and -ve supply $-V_{EE}$.

There are 2 types of dual supply

i) Balanced Dual supply

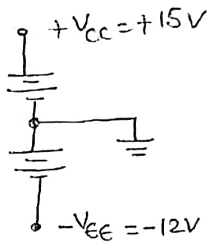
ii) unbalanced Dual supply

→ In Balanced dual supply, Both power supply voltages are same in magnitude i.e $+V_{cc} = +15V$, $-V_{EE} = -15V$.



Balanced dual supply

→ In unbalanced dual supply, both supply voltages magnitudes are not equal.



unbalanced dual supply

→ Practically in most of the op-amp circuits balanced power supply is used. and power supply ranges are ±9V, ±12V, ±22V etc..

→ To avoid the use of 2 separate power supplies, a single power supply is used.

→ There are various methods of obtaining dual supply from single supply.

i) From fig,

→ Each positive and negative supply has equal magnitude i.e equal to half of the single supply voltage used ($\frac{V_{in}}{2}$).

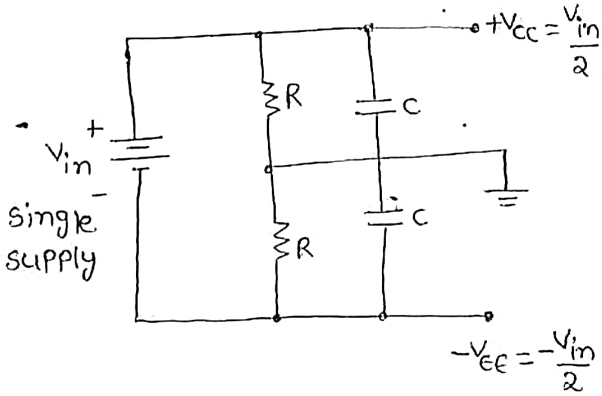


Fig:- obtaining dual supply from single supply

→ capacitors used to supply by passing i.e decoupling of power supply.

→ Resistors should not drawn high current from supply hence the values more than 10kΩ.

→ If the voltages required are other than $\frac{V_{in}}{2}$ then zener diodes are used for appropriate voltage rating.

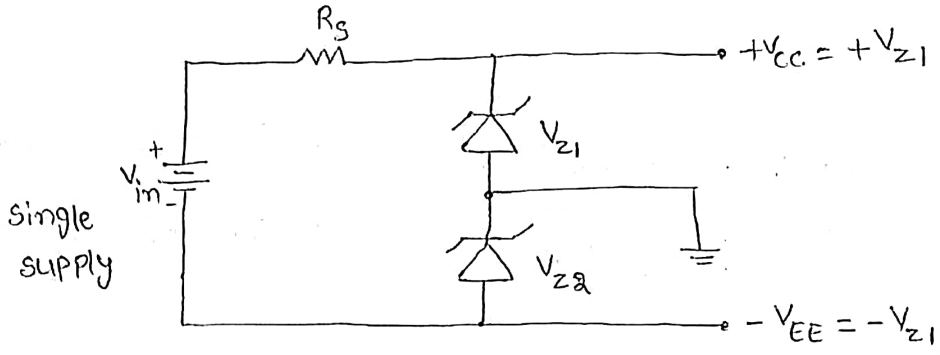


Fig :- use of zener diodes

→ many times practically due to mismatch in the devices, equal +ve and -ve voltages are not available. To adjust them we are using potentiometer.

→ To avoid damage due to reversal of polarities connected to IC, diodes D_1, D_2 used.

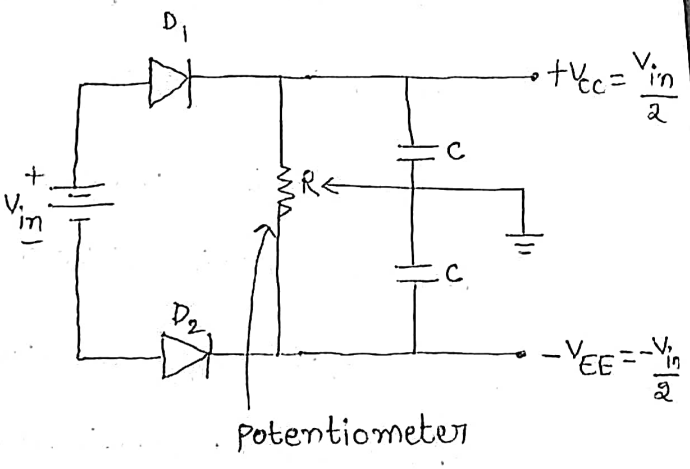


Fig :- use of potentiometer

Temperature ranges :-

There are 3 different temperature ranges

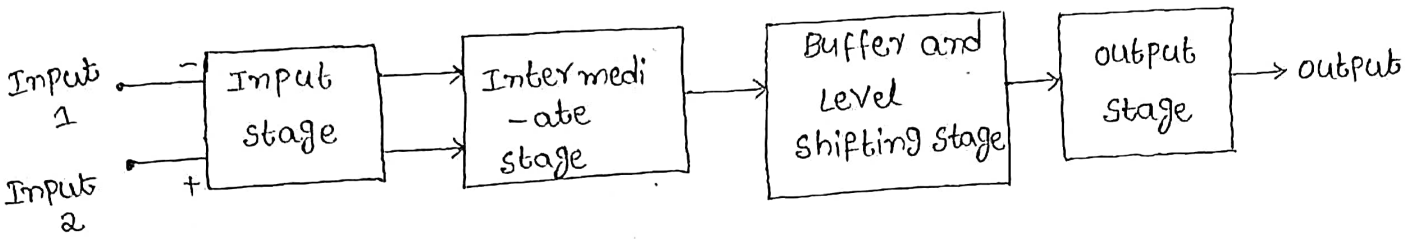
i) military temperature range → $-55^{\circ}c$ to $+125^{\circ}c$ ($-55^{\circ}c$ to $+85^{\circ}c$)

ii) Industrial temperature range → $-20^{\circ}c$ to $+85^{\circ}c$ ($-40^{\circ}c$ to $+85^{\circ}c$)

iii) commercial temperature range → $0^{\circ}c$ to $70^{\circ}c$ (or) ($0^{\circ}c$ to $+75^{\circ}c$)

Block diagram representation of OP-Amp :-

OP-Amps usually consists of 4 cascaded blocks.



1. Input Stage:-

→ In this stage using Dual Input Balanced output differential amplifier circuit. ie we are giving 2 Inputs and produces 2 outputs.

→ The function of differential Amplifier is used to Amplify the difference between 2 Input Signals.

→ High Input Impedance (or) high Input resistance is required and Low output resistance is required.

→ In this stage 2 Inputs are required they are Inverting & Non-Inverting terminals.

→ In the Inverting terminal (-) It requires 180° phase shift between Input and output.

→ In the Non-Inverting terminal (+), No phase shift is required between Input and output.

2. Intermediate stage :-

The output of the Input stages drives the next stage which is an Intermediate stage.

→ This stage is similar to Dual Input, unbalanced output i.e we are giving 2 Inputs and produces single output.

→ The main function of this stage is used to Increases the Gain Value.

→ Practically, the Intermediate stage is not a single amplifier it contains cascaded Amplifiers called multi stage Amplifiers.

Note :-

The concept of Intermediate stage is similar to the operation of cascaded differential Amplifier stages in unit-1.

3. Level shifting stage :-

All the stages are directly coupled to each other. The coupling capacitors are not used to cascade the stages. Hence the d.c ovuiescent voltage level of previous stage gets applied to Input to Next stage. Hence stage by stage d.c level Increases. As the d.c level Increases, it causes distortion in the output due to clipping. This may limit the maximum A.c output voltage swing with out any distortion

→ The Level shifter stage brings the d.c level down to ground potential, when no signal is applied at the Input.

→ The buffer is usually an Emitter follower whose Input Impedance is very high.

Note:-

Level shifting stage operation is similar to D.C translator operation in Unit-1.

4. output stage:-

→ The basic requirement of output stage is Low output resistance

→ The Push-Pull complementary Amplifier used an output stage.

→ This stage Increases the output voltage swing and keeps the voltage swing symmetrical with respect to ground.

→ The requirements of good output stage are

i) Large output voltage, current swing capability

ii) Low output Impedance

iii) Low Quiescent power dissipation

iv) short circuit protection

consider Push-Pull Amplifier in class B, which is basically Emitter-follower with complementary transistors.

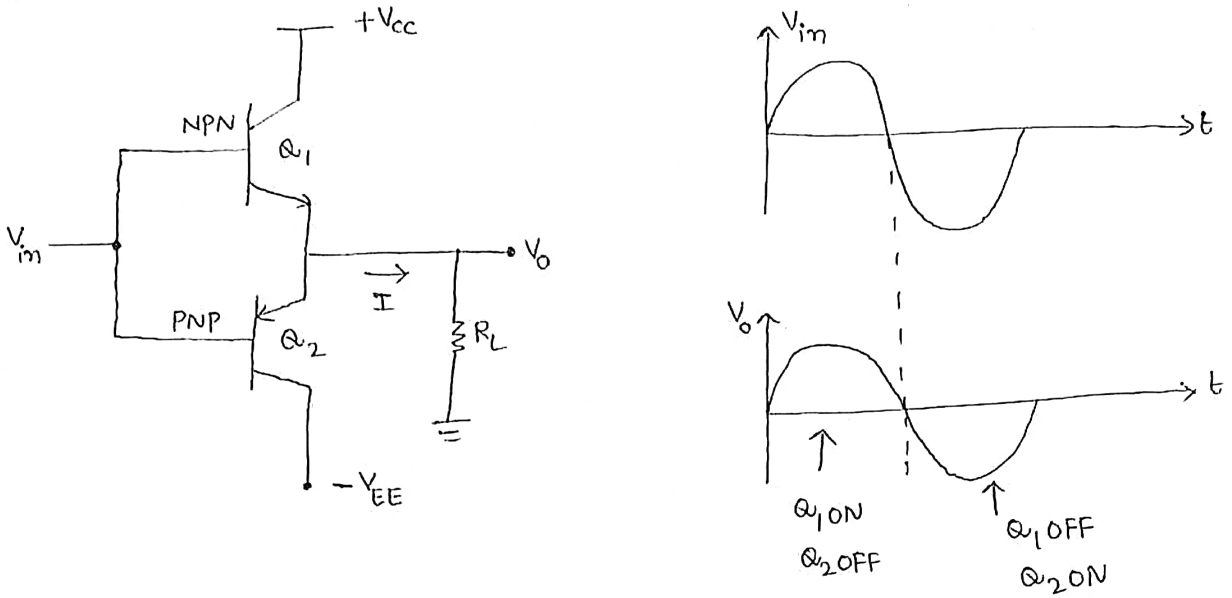


Fig :- output stage of an OP-Amp

→ when V_{in} is +ve, transistor Q_1 ON, Q_2 OFF.

Q_1 supplies the load.

→ when V_{in} is -ve, Q_1 OFF, Q_2 ON. Q_2 act as sink to remove the current from the load.

→ major limitation of the circuit is output voltage remains zero as V_{in} is less than V_{BE}. This Introduces the cross-over distortion in the output.

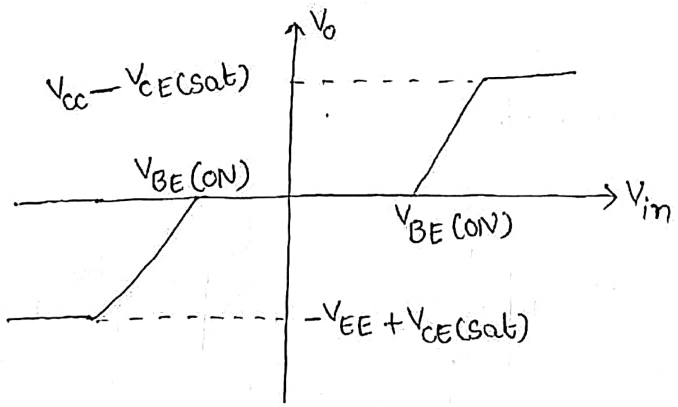


Fig :- cross over distortion in the output

Characteristics and performance specifications of OP-Amp :-

i) Input offset voltage :-

When ever both Input terminals of the op-amp are grounded, ideally the output voltage is zero but practically it has non-zero output voltage. This is due to mismatching present in the Internal circuit of op-amp.

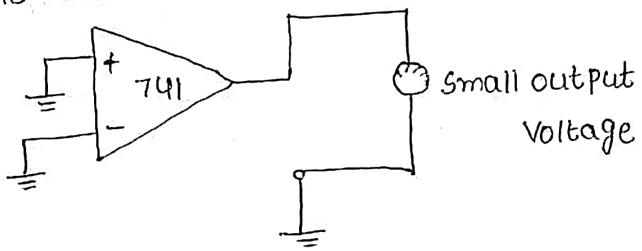
Def:-

The differential voltage that must be applied between 2 Input terminals of the op-Amp, to make the output voltage zero is called "Input offset voltage".

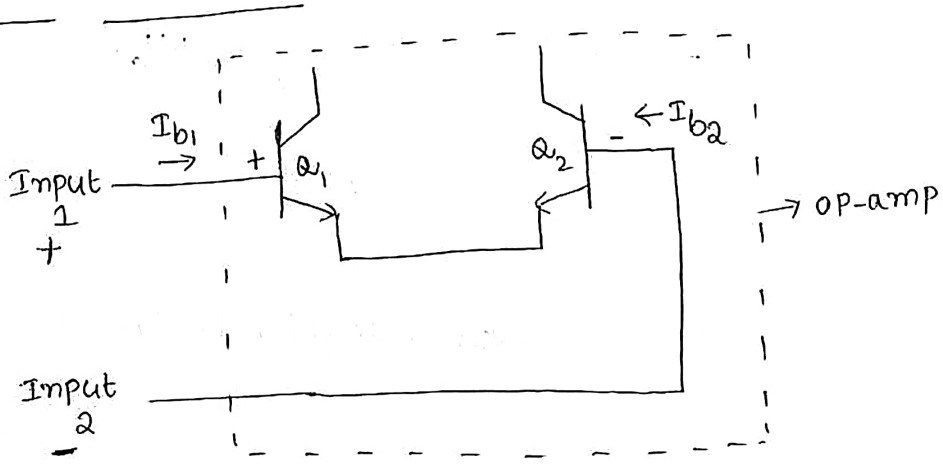
→ It is denoted as V_{ios}

→ practically for OP-amp 741C, the Input offset voltage is 6mV.

→ Ideally, V_{ios} is zero



ii) Input offset current :-



def :- The algebraic difference between the currents flowing into the two Input terminals of the op-amp is called "Input - offset current".

→ It is denoted by I_{ios}

→ mathematically, $\boxed{I_{ios} = |I_{b_1} - I_{b_2}|}$

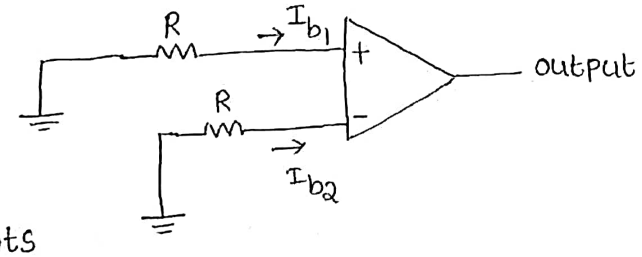
where, I_{b_1} → current entering into Non Inverting Input terminal

I_{b_2} → current entering into Inverting Input terminal

→ Practically, I_{ios} value is 200nA.

→ Ideally, I_{ios} is zero.

3. Input bias current :-



It is defined as the,

The Average value of two currents flowing into the op-amp input terminals is called "Input bias current".

→ It is denoted as I_b.

mathematically,

$$\boxed{I_b = \frac{I_{b_1} + I_{b_2}}{2}}$$

→ Ideally it should be zero, Practically for op-amp 741C, is 500nA.

4. Differential Input resistance :- (or) Input resistance :- (R_i)

It is the equivalent resistance measured at either the Inverting (or) Non-Inverting Input terminal with other Input terminal grounded.

→ It is denoted as R_i

→ Ideally, it should be Infinite Value

→ Practically, opamp 741C is order of 2 MΩ.

5. Input capacitance :- (C_i)

It is the equivalent capacitance measured at either the Inverting (or) Non-Inverting Input terminal with other Input terminal grounded.

→ It is denoted as C_i

→ Practically, for op-amp 741C, it is 1-4 PF.

6. open Loop Voltage gain :- (or) Large signal voltage gain (A_{OL}) :-

It is defined as the ratio of output voltage to the differential Input voltage, when op-amp is in open loop configuration with out any feed back.

$$A_{OL} = \frac{V_o}{V_d}$$

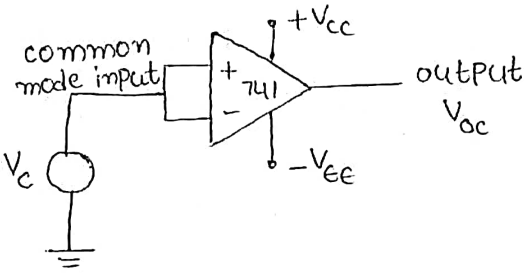
→ For opamp 741C, it is typically 2,00,000.

7. CMRR :-

It is the ratio of differential voltage gain (A_d) to the common mode voltage gain (A_c).

$$CMRR = \frac{A_d}{A_c}$$

A_d is nothing but open loop voltage gain A_{OL} & A_c is measured by using the circuit as shown in fig.



From fig,

common mode input V_c is applied to both Input terminals, output V_{oc} is measured.

Then, common mode gain $A_c = \frac{V_{oc}}{V_c}$

→ It is expressed in dB

→ For op-amp 741C it is 90dB.

8. output voltage swing :-

The op-amp output voltage gets saturated at $+V_{cc}$ and $-V_{EE}$ and it can not produce output voltage more than $+V_{cc}$ and $-V_{EE}$.

→ Practically, saturation voltages $+V_{sat}$ and $-V_{sat}$ are less than $+V_{cc}$ and $-V_{EE}$

→ For op-amp 741C, the saturation voltages are ±13V for supply voltages ±15V.

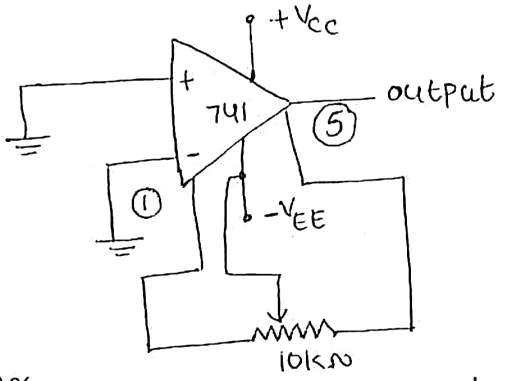
9. output resistance :-

It is the equivalent resistance measured between the output terminal of the op-amp and the ground.

→ It is denoted as R_o

→ For op-amp 741C it is 75Ω

10. offset voltage adjustment range :-



→ The pins 1 and 5 are offset null pins for op-amp 741.

→ A 10kΩ potentiometer can be connected to pin 1 and pin5.

→ The variable end of potentiometer is connected to $-V_{EE}$. By varying potentiometer, the output can be adjusted to zero.

def :- "The range for which input offset voltage can be adjusted using the potentiometer to reduce output to zero", is called offset voltage adjustment range.

→ For op-amp 741C, it is ±15mV.

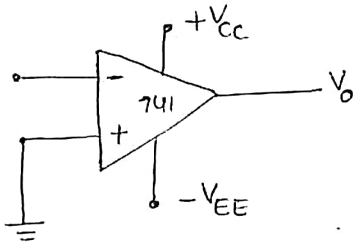
11. Input voltage range :-

It is the range of common mode voltages which can be applied for which op-amp functions properly.

→ This range also dependent on supply voltages.

→ For op-amp 741C, ±15V supply voltages, Input voltage range is ±13V.

12. Power Supply Rejection Ratio (PSRR) :-



It is defined as the "Ratio of change in input offset voltage due to change in supply voltage producing it, keeping other power supply voltage constant".

→ It is also called as Power Supply Sensitivity (PSV)

i) If V_{EE} is constant, V_{cc} is fixed then

$$PSRR = \left.\frac{\Delta V_{ios}}{\Delta V_{cc}}\right|_{V_{EE}=\text{constant}}$$

ii) If V_{cc} is constant, V_{EE} is fixed then

$$PSRR = \left.\frac{\Delta V_{ios}}{\Delta V_{EE}}\right|_{V_{cc}=\text{constant}}$$

→ PSRR is expressed in mV/V (or) μV/V

→ For IC 741 op-amp, PSRR is 30μV/V.

→ It also called as supply voltage rejection ratio (SVRR).

13. Power consumption :- (P_c)

It is the amount of Quiescent power to be consumed by op-amp with zero Input voltage.

→ For op-amp 741C, it is 85mw.

14. Slew rate :-

It is defined as the maximum rate of change of output voltage with time.

$$\text{Slew rate } (S) = \left.\frac{dV_o}{dt}\right|_{max} \quad \text{—①}$$

→ Slew rate is specified in V/μsec

→ It is specified by the op-amp in unity gain condition.

→ The slew rate is caused due to limited charging rate of the compensation capacitor and current limiting and saturation of the Internal stages of op-amp, when a high frequency large amplitude signal is applied.

The Internal capacitor voltage can not change Instantaneously

It is given by $\frac{dV_o}{dt} = \frac{I}{C}$ —② $\left[\because V_o = \frac{1}{C}\int i\,dt \quad \frac{dV_o}{dt} = \frac{i}{C}\right]$

From eq ②, Small value of 'C', current value large.

$$\therefore S = \frac{I_{max}}{C}$$

FOR IC741,

The charging current is 15μA and the Internal capacitor is 30PF. $S = 0.5\,V/\mu sec$

Slew rate equation :-

consider $V_s = V_m \sin\omega t$

$V_o = V_m \sin\omega t$

$\frac{dV_o}{dt} = V_m \omega \cos\omega t$

slew rate (S) $= \left.\frac{dV_o}{dt}\right|_{max}$

$S = V_m \omega$ [$\because$ for max, $\cos\omega t = 1$]

$\boxed{S = 2\pi f V_m \text{ V/sec}}$ —③

For distortion free output, the max. allowable input frequency f_m,

from eq ③, $\boxed{f_m = \frac{S}{2\pi V_m}}$

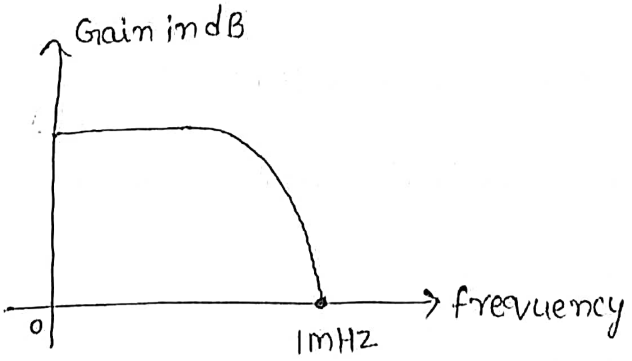
15. Gain - Band width product :-

It is the band width of op-amp when voltage gain is unity.

It is denoted as GB.

→ Gain is Expressed in dB, so unity gain has dB value $20 \log 1 = 0$dB

→ It also called unity gain band width (UGB) (or) closed loop Band width.



From the graph, gain reduces, frequency Increases.

16. Equivalent Input Noise voltage and current :-

The Noise is random in nature, hence it expressed as a power density.

→ The equivalent Noise voltage is expressed as V^2/Hz, equivalent noise current is expressed as A^2/Hz.

17. Average temperature coefficient of offset Parameters :-

→ The Average rate of change of Input offset voltage per unit change in temperature is called Average temperature coefficient of Input offset voltage (or) Input off set Voltage drift.

→ It is measured in $\mu V/^\circ C$. For 741 C it is $0.5 \mu V/^\circ C$

→ The average rate of change of Input offset current per unit change in temperature is called Average temperature coefficient of Input off set current (or) Input offset current drift.

→ It is measured in $nA/^\circ C$ (or) $PA/^\circ C$. For 741C it is $12 PA/^\circ C$

18. output offset voltage (V_{oos}) :-

The output offset voltage is the dc voltage present at the output terminals when both the Input terminals are grounded.

→ It is denoted as V_{oos}.

19. Supply current:-

It is the current drawn by the op-amp from the power -supply.

→ For op-amp 741C it is 2.8 mA

Transient response Rise time :-

when the output of the op-amp is suddenly changing like pulse type, then rise time of the response depends on the cut-off frequency f_H of the op-amp. Such rise time is called cut-off frequency limited rise time (or) transient response rise time.

$$t_r = \frac{0.35}{f_H}$$

D.c characteristics of op-Amp :-

The Important d.c characteristics are

i) Input bias current (I_b)

ii) Input off set current (I_{ios})

iii) Input offset voltage (V_{ios})

iv) Thermal drift

4. Thermal drift:-

The op-amp parameters input off set current, Input off set voltage, Input bias current are not constant but vary with the factors : i) Temperature ii) change in supply

voltage iii) Time

The effect of change in temperature on the parameters is most severe.

i) Effect on Input offset voltage :-

It is defined as the average rate of change of Input offset voltage per unit change in temperature.

→ It is also called as Input offset voltage drift.

$$\text{Input offset voltage drift} = \frac{\Delta V_{ios}}{\Delta T}$$

where,

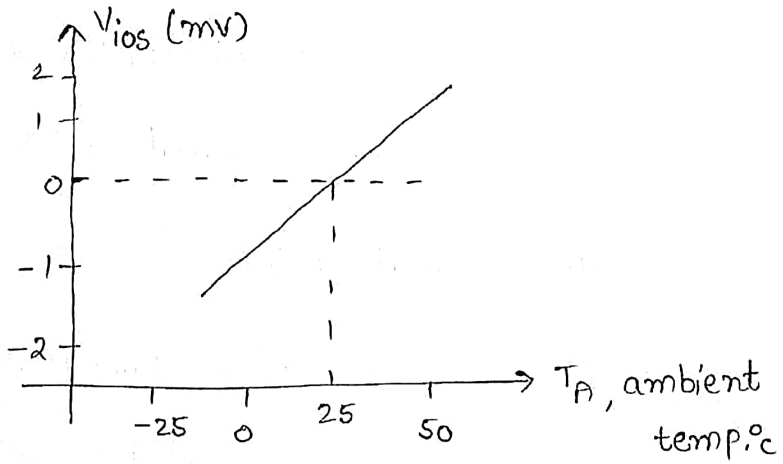
ΔV_{ios} → change in Input offset voltage

ΔT → change in temperature

→ It is expressed in $\mu V/^{\circ}C$.

→ The drift is not constant and it is not uniform over specified operating temperature range.

→ The value of Input offset voltage may Increase (or) decrease with Increasing temperature.



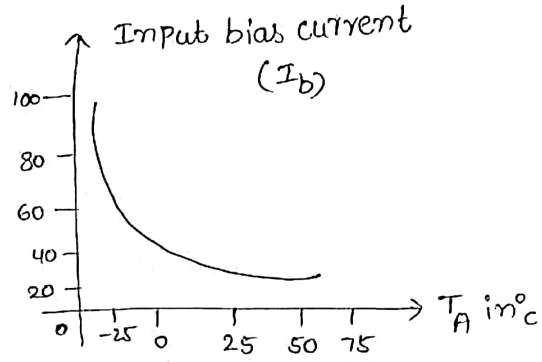
ii) Effect on Input bias current drift :-

It is defined as the average rate of change of Input bias current per unit change in temperature.

$$\text{Thermal drift in Input bias current} = \frac{\Delta I_b}{\Delta T}$$

→ It is measured in nA/°c (or) pA/°c

→ These parameters vary randomly with temperature i.e they may be +ve in one temperature range and -ve in other temperature range



iii) Effect on Input offset current drift :-

It is defined as the average rate of change of Input offset current per unit change in temperature.

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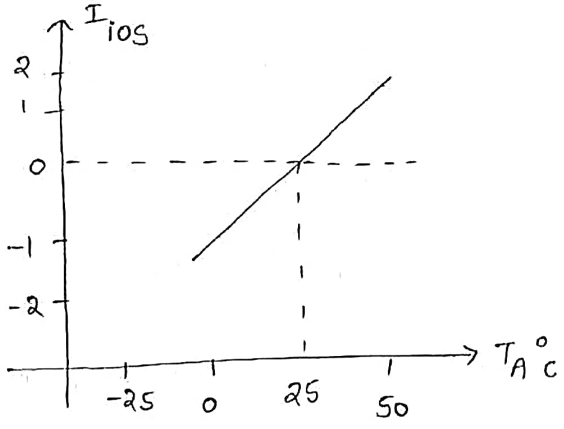


A.c characteristics :-

mainly there are

1. Frequency response
2. slew rate
3. stability of an op-amp

1. Frequency response :-

Ideally, an op-amp should have Infinite bandwidth but practically, op-amp gain decreases with Increase in temperature such a gain reduction with respect to frequency is called roll off.

→ The plot showing the variations in magnitude and phase angle of the gain due to change in frequency is called frequency response of op-amp.

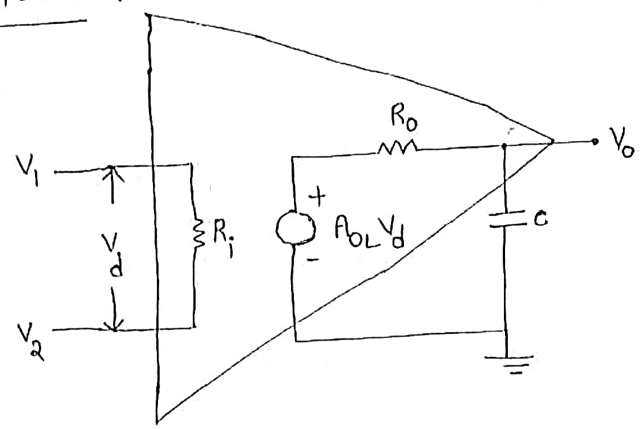
→ when the gain in decibels (dB), phase angle in degrees are plotted against Logarithmic scale of frequency, the plot is called "Bode plot".

→ Gain of the op-amp changes with variation in frequency is called "magnitude plot".

→ Phase shift changes with change in frequency is called "phase angle plot".

Obtaining frequency response :-

To obtain frequency response, consider the high frequency model of op-amp with capacitor 'c' at the output.



Let $-jx_c$ be the capacitive reactance.

using voltage divider rule,

$$V_o = \frac{-jx_c}{R_o - jx_c} \cdot A_{OL} V_d$$

Let $-j = \frac{1}{j}$, $X_c = \frac{1}{2\pi fc}$

$$\Rightarrow V_o = \frac{\frac{1}{j2\pi fc}}{R_o + \frac{1}{j2\pi fc}} \cdot A_{OL} V_d$$

$$\Rightarrow V_o = \frac{1}{R_o(j2\pi fc) + 1} \cdot A_{OL} V_d$$

$$\Rightarrow \frac{V_o}{V_d} = \frac{A_{OL}}{1 + j2\pi f R_o c}$$

$$\Rightarrow \boxed{A_{OL}(f) = \frac{A_{OL}}{1 + j2\pi f R_o c}} \quad -(1)$$

consider $f_o = \frac{1}{2\pi R_o c}$

$$\Rightarrow \boxed{A_{OL}(f) = \frac{A_{OL}}{1 + j(f/f_o)}} \quad -(2)$$

19. Supply current:-

It is the current drawn by the op-amp from the power -supply.

→ For op-amp 741C it is 2.8 mA

Transient response Rise time :-

when the output of the op-amp is suddenly changing like pulse type, then rise time of the response depends on the cut-off frequency f_H of the op-amp. Such rise time is called cut-off frequency limited rise time (or) transient response rise time.

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The op-amp parameters input off set current, Input off set voltage, Input bias current are not constant but vary with the factors : i) Temperature ii) change in supply

voltage iii) Time

The effect of change in temperature on the parameters is most severe.

i) Effect on Input offset voltage :-

It is defined as the average rate of change of Input offset voltage per unit change in temperature.

→ It is also called as Input offset voltage drift.

$$\text{Input offset voltage drift} = \frac{\Delta V_{ios}}{\Delta T}$$

where,

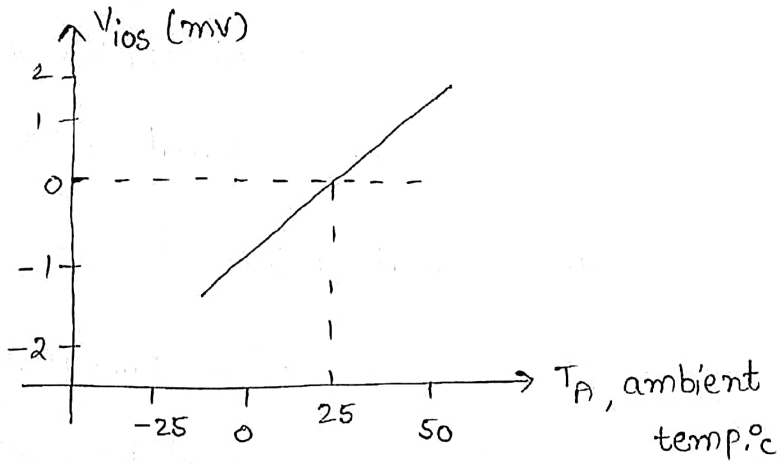
ΔV_{ios} → change in Input offset voltage

ΔT → change in temperature

→ It is expressed in $\mu V/^{\circ}C$.

→ The drift is not constant and it is not uniform over specified operating temperature range.

→ The value of Input offset voltage may Increase (or) decrease with Increasing temperature.



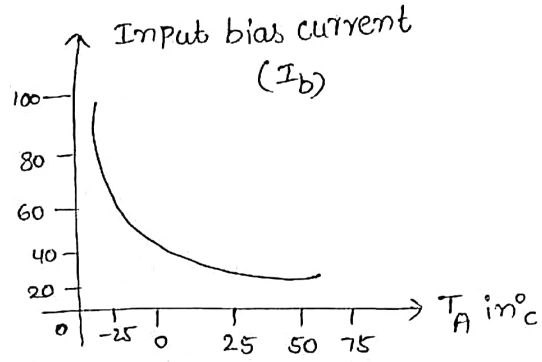
ii) Effect on Input bias current drift :-

It is defined as the average rate of change of Input bias current per unit change in temperature.

$$\text{Thermal drift in Input bias current} = \frac{\Delta I_b}{\Delta T}$$

→ It is measured in nA/°c (or) pA/°c

→ These parameters vary randomly with temperature i.e they may be +ve in one temperature range and -ve in other temperature range



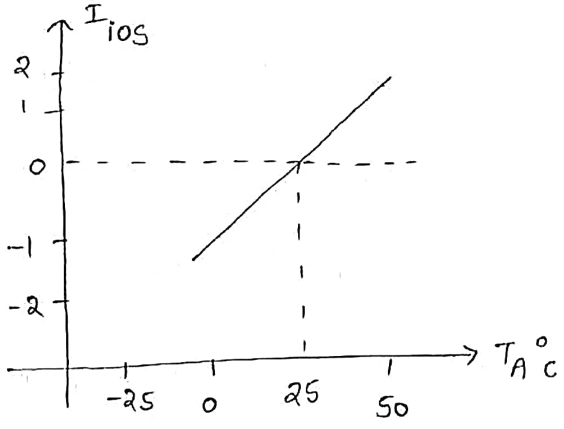
iii) Effect on Input offset current drift :-

It is defined as the average rate of change of Input offset current per unit change in temperature.

$$\text{Thermal drift in Input offset current} = \frac{\Delta I_{ios}}{\Delta T}$$

→ It is measured in nA/°c (or) pA/°c

→ These parameters vary randomly with temperature i.e they may be +ve in one temperature range and -ve in other.



A.c characteristics :-

mainly there are

1. Frequency response
2. slew rate
3. stability of an op-amp

1. Frequency response :-

Ideally, an op-amp should have Infinite bandwidth but practically, op-amp gain decreases with Increase in temperature such a gain reduction with respect to frequency is called roll off.

→ The plot showing the variations in magnitude and phase angle of the gain due to change in frequency is called frequency response of op-amp.

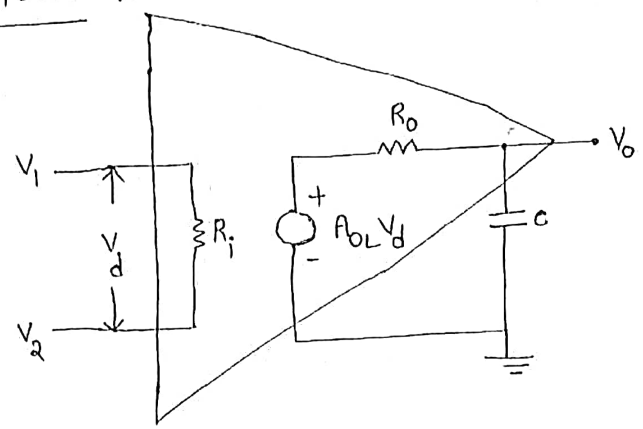
→ when the gain in decibels (dB), phase angle in degrees are plotted against Logarithmic scale of frequency, the plot is called "Bode plot".

→ Gain of the op-amp changes with variation in frequency is called "magnitude plot".

→ Phase shift changes with change in frequency is called "phase angle plot".

Obtaining frequency response :-

To obtain frequency response, consider the high frequency model of op-amp with capacitor 'c' at the output.



Let $-jx_c$ be the capacitive reactance.

using voltage divider rule,

$$V_o = \frac{-jx_c}{R_o - jx_c} \cdot A_{OL} V_d$$

Let $-j = \frac{1}{j}$, $X_c = \frac{1}{2\pi fc}$

$$\Rightarrow V_o = \frac{\frac{1}{j2\pi fc}}{R_o + \frac{1}{j2\pi fc}} \cdot A_{OL} V_d$$

$$\Rightarrow V_o = \frac{1}{R_o(j2\pi fc) + 1} \cdot A_{OL} V_d$$

$$\Rightarrow \frac{V_o}{V_d} = \frac{A_{OL}}{1 + j2\pi f R_o c}$$

$$\Rightarrow \boxed{A_{OL}(f) = \frac{A_{OL}}{1 + j2\pi f R_o c}} \quad -(1)$$

consider $f_o = \frac{1}{2\pi R_o c}$

$$\Rightarrow \boxed{A_{OL}(f) = \frac{A_{OL}}{1 + j(f/f_o)}} \quad -(2)$$

where,

$A_{OL}(f)$ = open loop voltage gain as a function of frequency

A_{OL} = Gain of the OP-amp

f = operating frequency

f_o = Break frequency (or) cut-off frequency

eq ② can be written in magnitude and Polar form,

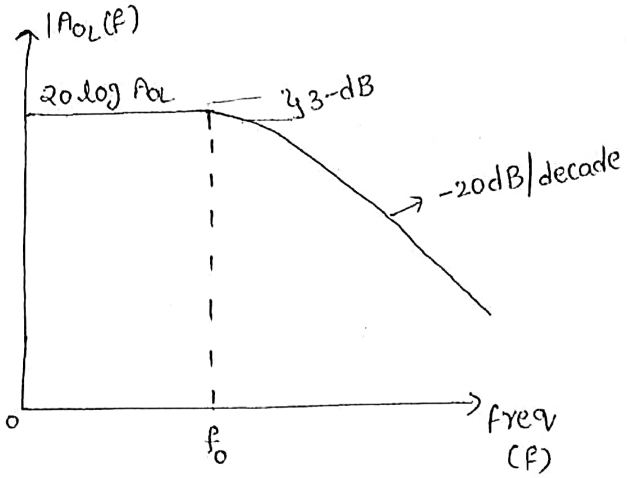
i.e magnitude $\rightarrow |A_{OL}(f)| = \frac{A_{OL}}{\sqrt{1+\left(\frac{f}{f_o}\right)^2}}$

phase angle $\rightarrow \angle A_{OL}(f) = \phi(f) = -\tan^{-1}\left(\frac{f}{f_o}\right)$

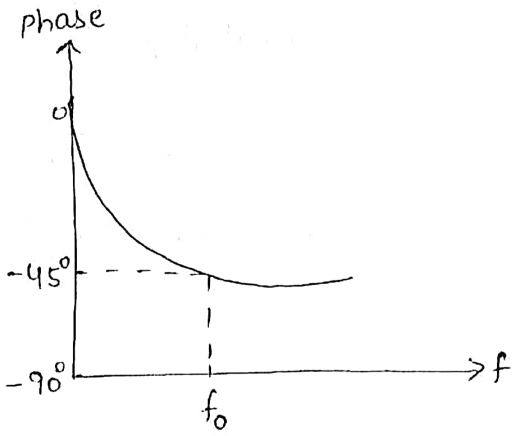
FOR IC741 OP-amp,

$f_o = 5Hz$, open LOOP gain 2,00,000 caluclate magnitude and phase shifts at various frequencies as show in table below.

frequency in Hz	$\lvert A_{OL}(f)\rvert = 20\log \frac{A_{OL}}{\sqrt{1+(f/f_o)^2}}$ in decibles (dB)	$\phi(f) = -\tan^{-1}\left(\frac{f}{f_o}\right)$ in degrees
0	106.02 dB	0°
5	103.01 dB	-45°
10	99.03 dB	-63.43°
100	79.98 dB	-87.13°
1000	60.00 dB	-89.71°
100×10^3	20.00 dB	-89.99°
1×10^6	0dB	-89.999°



a) magnitude characteristics



b) phase characteristics

From the graph

i) open loop gain A_{OL} is constant from 0Hz to break freq. f_0

ii) At $f=f_0$, gain is 3dB down from its value at 0Hz.

Hence f_0 is also called -3dB frequency (or) corner frequency

iii) After $f=f_0$, gain decreases, slope of the magnitude plot is -20dB/decade (or) -6dB/octave, after $f=f_0$.

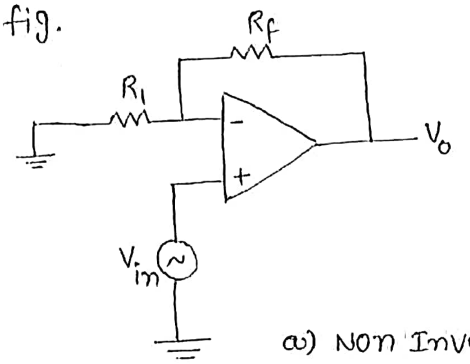
iv) At certain frequency, gain reduces to 0dB. i.e $20 \log |A_{OL}|$ is 0dB i.e $|A_{OL}|=1$. Such frequency is called gain cross-over frequency (or) unity gain bandwidth (UGB) (or) closed loop band width.

2. Slew rate :-

*Note :- Previously discussed to refer that.

3. Stability of an OP-amp :-

consider non Inverting amplifier with resistive feed back as shown in fig.



a) Non Inverting Amplifier

→ The block between Input and output is called forward block.

→ The block between output signal and feed back is called feed back block.

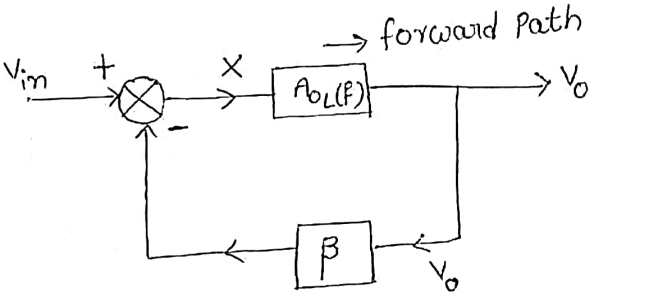


Fig :- Block diagram of Non-Inverting Amplifier

From fig, $X = V_{in} - \beta V_o$ — ①

and $V_o = X[A_{OL(F)}]$

$$\Rightarrow X = \frac{V_o}{A_{OL(F)}} \quad \text{— ②}$$

Sub. eq ② in ①

$$\Rightarrow \frac{V_o}{A_{OL(F)}} = V_{in} - \beta V_o$$

$$\Rightarrow \frac{V_o}{A_{OL(F)}} + \beta V_o = V_{in} \quad \Rightarrow V_o\left[\frac{1}{A_{OL(F)}} + \beta\right] = V_{in}$$

$$\Rightarrow \frac{V_o}{V_{in}} = \frac{A_{OL}(f)}{1+A_{OL}(f)\beta} \quad \text{—(3)} \qquad \left[\because \frac{V_o}{V_{in}} = \frac{1}{A_{OL}(f)} + \beta = \frac{1+\beta A_{OL}(f)}{A_{OL}(f)} \right]$$

eq(3) called closed loop gain.

The characteristic equation of system is given by

$$1 + A_{OL}(f)\beta = 0$$

$$\Rightarrow A_{OL}(f)\beta = -1 \quad \text{—(4)}$$

eq(4) expressed in complex form as

$$A_{OL}(f)\beta = -1 + j.0 \quad \text{—(5)}$$

The magnitude and phase angles given by

$$|A_{OL}(f)\beta| = \sqrt{1^2+0^2}$$

$$\Rightarrow |A_{OL}(f)\beta| = 1 \quad \text{—(6)}$$

and $\angle A_{OL}(f)\beta = \tan^{-1}\left(\frac{0}{1}\right)$

$= 0^\circ$ (or) $2n\pi$ radians. —(7)

eq(6), (7) are called Barkhausen criterion for the sustained oscillations.

Stability specifications :-

i) Gain cross over frequency (ω_{gc}) :-

The frequency at which the loop gain magnitude $|A_{OL}(f)\beta| = 1$ i.e $20\log|A_{OL}(f)\beta| = 0$ dB is called gain cross over frequency.

ii) Phase cross over frequency (ω_{pc}) :-

The frequency at which the phase shift Introduced by the loop gain is -180° (or) $n\pi$ radians is called phase cross over frequency.

iii) Gain margin (G.M) :-

The gain measured at the frequency $\omega = \omega_{p.c}$ is called gain margin. so, Loop gain $|A_{OL}(f)\beta|$ measured at $\omega = \omega_{p.c}$

mathematically,

$$G.M = -20 \log |A_{OL}(f)\beta|_{\omega=\omega_{pc}} \quad dB$$

iv) Phase margin (P.M) :-

The amount by which angle of loop gain $\angle A_{OL}(f)\cdot\beta$ differ from the -180° phase shift, at $\omega = \omega_{gc}$ is called phase margin.

mathematically,

$$P.M = 180^\circ + \angle A_{OL}(f)\beta|_{\omega=\omega_{gc}}$$

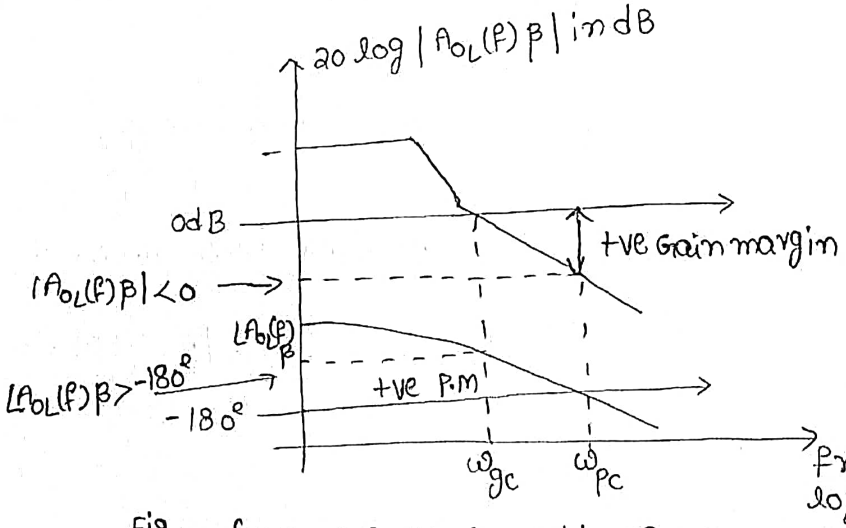


Fig:- freq. response of stable OP-amp

Measurement techniques of op-amp Parameters

1. measurement of open loop voltage gain (A_{OL}) :-

It is defined as the ratio of output voltage to the input differential voltage.

→ It is normally specified at a.c with an output voltage swing of ±10V across the load, with the amplifier working at ±15V power supply.

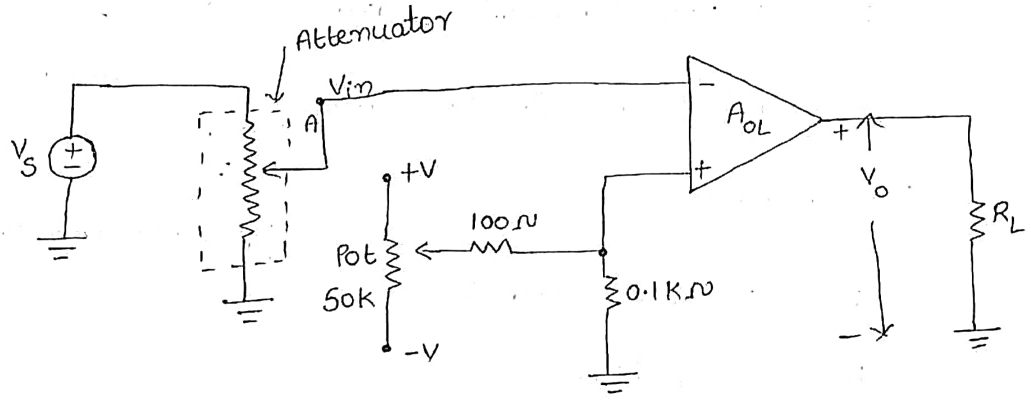


Fig:- measurement of open loop voltage gain

→ The source signal is attenuated by 40dB i.e reduced by $\frac{1}{100}$ before applying V_S, the output offset voltage is compensated using resistive network connected to non Inverting Input terminal.

From fig, $\boxed{A_{OL} = \frac{V_o}{V_{in}}}$

2. measurement of Input bias current :-

It is defined as the Average of currents that flow into Inverting and Non Inverting terminals of the op-amp.

$$I_b = \frac{I_{b1} + I_{b2}}{2}$$

→ The op-amp is used in the closed loop configuration

→ The 2-Input currents I_{b1} and I_{b2} flowing through resistances like 7.2 mΩ.

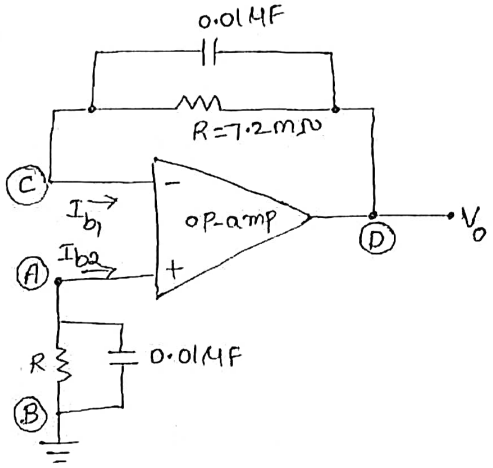


Fig:- measurement of Input bias current

→ The capacitors used to elimantes noise.

The steps used for the measurements are

1. short A and B :-

Due to this, A gets grounded.

Now I_{b1} flows through resistance R, output voltage is V_{01}.

$$\Rightarrow V_{01} = I_{b1} R$$

$$\boxed{I_{b1} = \frac{V_{01}}{R}}$$

2. short C and D :-

In this case I_{b2} flows through resistor R, output voltage is V_{02}. $\Rightarrow V_{02} = I_{b2} R \Rightarrow \boxed{I_{b2} = \frac{V_{02}}{R}}$

3. measurement of Input offset current :-

It is defined as the difference between 2 currents flows through it.

$$I_{ios} = |I_{b1} - I_{b2}|$$

Note :- The circuit and measurement is similar to Input bias current.

4. measurement of Input offset voltage and PSRR :-

It is defined as the voltage applied between Input terminals to get zero output voltage.

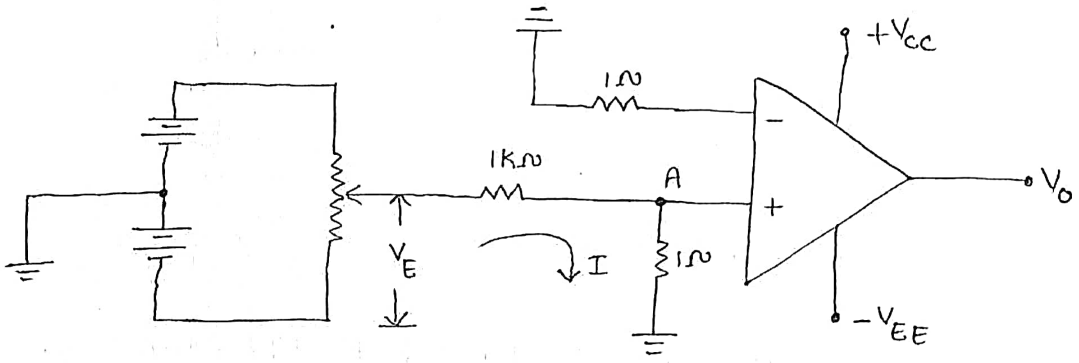


Fig :- measurement of V_{ios} and PSRR

The OP-amp is dual supply is adjusted to exact ±10v.

The potentiometer is used to adjust output voltage to zero.

From fig, $I = \frac{V_E}{1K\Omega + 1\Omega} \approx \frac{V_E}{1000}$

and $V_A = I \times 1\Omega = \frac{V_E}{1000}$

Input offset voltage applied to Non-Inverting terminal to get zero output.

$$\therefore \boxed{V_{ios} = V_A = \frac{V_E}{1000}}$$

→ same circuit is used to measure PSRR. (Power supply rejection ratio)

It is defined as the ratio of change in input offset voltage to change in supply voltage by keeping other supply as constant.

$$\text{i.e } PSRR = \left.\frac{\Delta V_{ios}}{\Delta V_{cc}}\right|_{V_{EE}=\text{const.}}$$

(or)

$$PSRR = \left.\frac{\Delta V_{ios}}{\Delta V_{EE}}\right|_{V_{cc}=\text{constant}}$$

→ From fig, supply is ±10V

i) −10V is constant (V_{EE}) :-

In this case $+V_{cc}$ changed to +9V from +10V. again V_E adjusted to get output voltage as zero, corresponding V_A measured which is consider as V_{ios1}. Then $+V_{cc}$ changed to +11V again V_E adjusted to get output voltage to zero. corresponding V_A is V_{ios2}. Then PSRR,

$$PSRR = \frac{\Delta V_{ios}}{\Delta V_{cc}} = \frac{V_{ios2} - V_{ios1}}{11-9} = \frac{V_{ios2} - V_{ios1}}{2}$$

ii) +10V is constant (V_{cc}) :- change V_{EE} from −9 to −11V and measure V_A.

PSRR corresponding to -Ve supply can be measured.

5. measurement of CMRR :-

It is defined as the ratio of differential gain to common mode gain.

→ The common mode signal V_s is applied to both Inputs.

i.e $A_c = \frac{V_o}{V_s}$

and $V_d = V_B - V_A$ —①

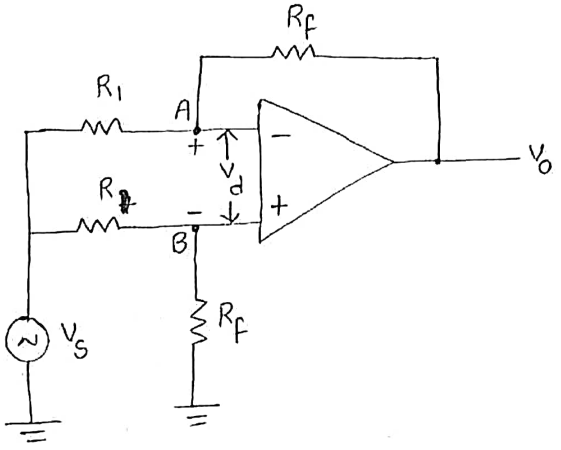


Fig :- measurement of CMRR

Now

$$V_B = \frac{V_s \cdot R_1}{R_1 + R_f} \quad —②$$

To calculate V_A, use super position principle, as V_A due to 2 voltages V_s and V_o.

V_o grounding → $V_{A1} = \frac{R_f}{R_1 + R_f} \cdot V_s$

R_1 as grounding → $V_{A2} = \frac{R_1}{R_1 + R_f} \cdot V_o$

$$\Rightarrow V_A = V_{A1} + V_{A2}$$

$$= \frac{R_f V_s}{R_1 + R_f} + \frac{R_1 V_o}{R_1 + R_f} \quad —③$$

substitute eqn ②, ③ in ①

$$\Rightarrow V_d = \frac{V_s R_1}{R_1 + R_f} - \frac{R_f V_s}{R_1 + R_f} - \frac{R_1 V_o}{R_1 + R_f}$$

$$\Rightarrow V_d = \frac{V_S R_f - V_S R_f - V_o R_1}{R_1 + R_f}$$

$$\Rightarrow V_d = \frac{-V_o R_1}{R_1 + R_f} \qquad \Rightarrow \frac{V_d}{V_o} = \frac{-R_1}{R_1 + R_f}$$

$$\Rightarrow \frac{V_o}{V_d} = -\frac{R_1 + R_f}{R_1}$$

$$\Rightarrow A_d \doteq -\left[1 + \frac{R_f}{R_1}\right]$$

By knowing values of R_1, R_f, magnitude of A_d can be obtained.

Hence, CMRR can be measured as

$$\boxed{CMRR = \frac{|A_d|}{|A_c|}}$$

6. measurement of output offset voltage :-

It is defined as the difference between d.c voltage present at the output terminals when both Input terminals are grounded.

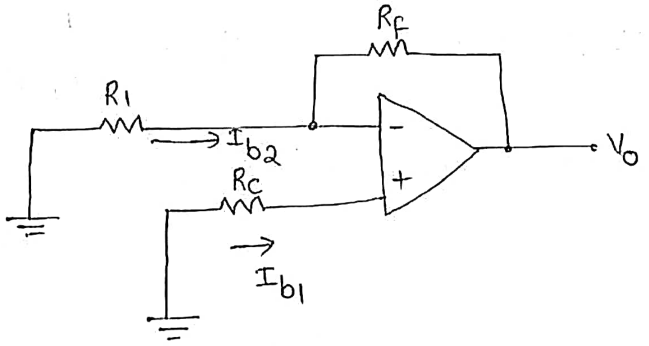


Fig :- measurement of output offset voltage

From fig,

output voltage due to I_{b2} is,

$$V_{o1} = I_{b2} R_1 \left(\frac{-R_f}{R_1}\right) \quad \text{—①}$$

output voltage due to I_{b1} is,

$$V_{o2} = I_{b1} R_c \left(1 + \frac{R_f}{R_1}\right)$$

Practically, R_c is selected equal to R_1

$$\Rightarrow V_{o2} = I_{b1}(R_1 + R_f) \quad -②$$

From eq ①, ②

$$V_{o1} + V_{o2} = -I_{b2} R_f + I_{b1} R_1 + I_{b1} R_f$$

consider $R_1 << R_f$, neglect $I_{b1} R_1$ term

$$= -I_{b2} R_f + I_{b1} R_f$$

$$= R_f (I_{b1} - I_{b2}) = R_f \cdot I_{ios}$$

where I_{ios} is the magnitude of difference between 2 I/P currents.

while output voltage due to Input offset voltage is given by $V_{ios}\left(1 + \frac{R_f}{R_1}\right)$.

Total output offset voltage is given by

$$\boxed{V_{oos} = V_{ios}\left(1 + \frac{R_f}{R_1}\right) + I_{ios} R_f}$$

The voltage may be +ve (or) -ve

Frequency compensation techniques :-

The OP-amp circuit with single break (or) corner frequency is Inherently stable.

consider the system with three break (or) corner frequencies. This is possible Inpractice due to capacitive

component produced by No. of stages.

The open-loop transfer function is given by

$$A_{OL}(f) = \frac{A_{OL}}{\left(1+j\left(\frac{f}{f_1}\right)\right)\left(1+j\left(\frac{f}{f_2}\right)\right)\left[\left(1+j\left(\frac{f}{f_3}\right)\right)\right]} \quad ; \; 0<f_1<f_2<f_3$$

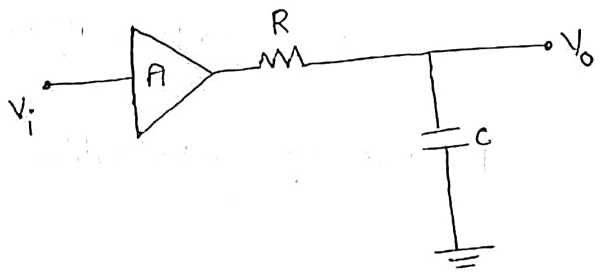
Frequency compensation techniques

- External compensation
  - Dominant pole compensation
  - Pole-zero compensation
- Internal compensation

1. External compensation :-

The compensating network is connected to the system Externally.

i) Dominant pole compensation :-



The compensated transfer function $A' = \frac{V_o}{V_i}$

$$= \frac{-jX_C}{R-jX_C} \cdot A$$

$$= \frac{\frac{1}{j2\pi fc}}{R+\frac{1}{j2\pi fc}} \cdot A$$

$$\left[\because \; -j = \frac{1}{j}, \quad X_C = \frac{1}{2\pi fc}\right]$$

$$A' = \frac{\frac{1}{j2\pi fC}}{\frac{R(j2\pi fC)+1}{j2\pi fC}} \cdot A$$

$$= \frac{1}{1+j2\pi fRC} \cdot A$$

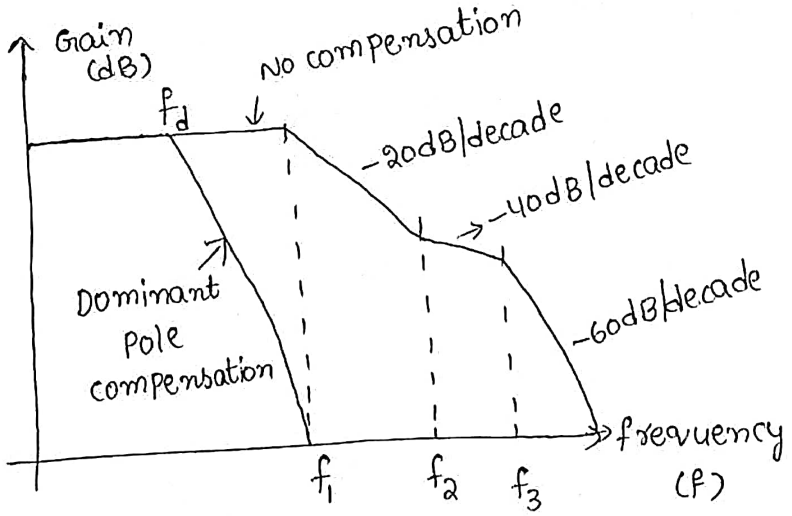
$$\Rightarrow \boxed{A' = \frac{A}{1+j\left(\frac{f}{f_d}\right)}} \qquad \left(\because \text{consider } f_d = \frac{1}{2\pi RC}\right)$$

$f_d \rightarrow$ break frequency (or) corner frequency

$$\Rightarrow A' = \frac{A_{OL}}{\left[1+j\left(\frac{f}{f_d}\right)\right]\left[1+j\left(\frac{f}{f_1}\right)\right]\left[1+j\left(\frac{f}{f_2}\right)\right]\left[1+j\left(\frac{f}{f_3}\right)\right]}$$

where $f_d < f_1 < f_2 < f_3$

The values of R and C are selected in such a way that loop gain drops to 0 dB with slope of -20dB/decade and at a frequency where the poles of uncompensated system contributes very small phase shift.



Advantage :-

To adjust f_d value, adequate phase margin and stability of system is assured.

disadvantage

→ Band width reduces.

ii) Pole-zero compensation :-

In this method, transfer function 'A' is modified by adding a pole and a zero with help of compensating network.

→ The zero added at higher frequency

→ Pole added at lower frequency.

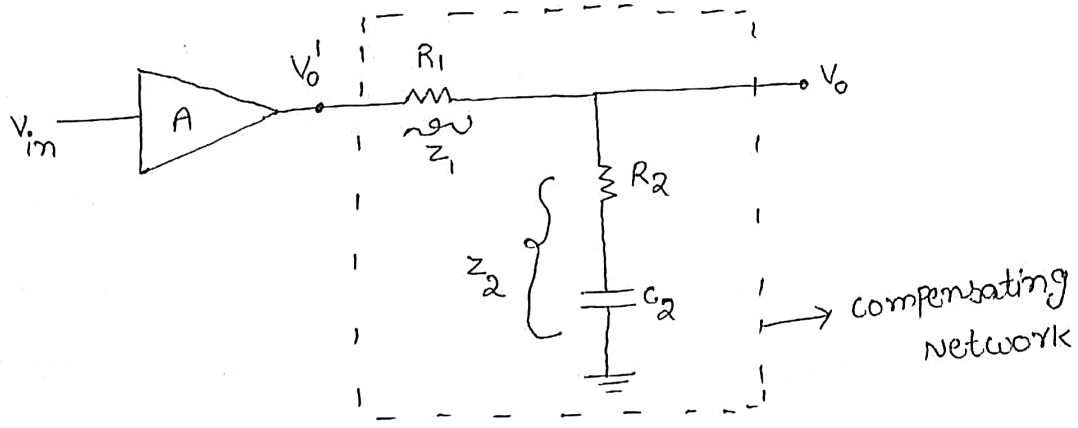


Fig :- Pole-zero compensation

Apply voltage divider rule,

$$V_o = \frac{Z_2}{Z_1+Z_2} \cdot V_o'$$

where, $Z_2 = R_2 - jX_{C_2}$

$$Z_1 = R_1$$

$$\Rightarrow V_o = \frac{R_2 - jX_{C_2}}{R_1 + R_2 - jX_{C_2}} \cdot V_o'$$

$$\Rightarrow \frac{V_o}{V_o'} = \frac{R_2 - jX_{C_2}}{R_1 + R_2 - jX_{C_2}}$$

$$\Rightarrow \quad \frac{V_o}{V_o'} = \frac{R_2 + \frac{1}{j2\pi f C_2}}{R_1 + R_2 + \frac{1}{j2\pi f C_2}} \qquad \left[\because \; -j = \frac{1}{j}, \quad X_{C_2} = \frac{1}{2\pi f C_2} \right]$$

$$A' = \frac{R_2 (j2\pi f C_2) + 1}{(R_1 + R_2) j2\pi f C_2 + 1} \quad \text{—— (1)}$$

consider $f_1 = \frac{1}{2\pi R_2 C_2}$ and

$$f_o = \frac{1}{2\pi (R_1 + R_2) C_2}$$

Then eq (1), becomes

$$\boxed{A' = \frac{1 + j\left(\frac{f}{f_1}\right)}{1 + j\left(\frac{f}{f_o}\right)}} \quad \text{—— (2)}$$

The values of R_1, R_2, C_2 are selected that break frequency for the zero matches with 1st corner frequency f_1 of the uncompensated system. while pole of the compensating Network f_o is selected in a such a way that compensated transfer function A' passes through 0 dB at 2nd corner frequency f_2 of the uncompensated system.

Loop gain becomes $A' = AA_1$

consider $A' = \frac{V_o}{V_i}$

$$= \frac{V_o}{V_o'} \cdot \frac{V_o'}{V_i} \quad \text{—— (3)}$$

Substitute eq ② in eq ③

$$A' = \left[\frac{1+j\left(\frac{f}{f_1}\right)}{1+j\left(\frac{f}{f_0}\right)}\right] . A$$

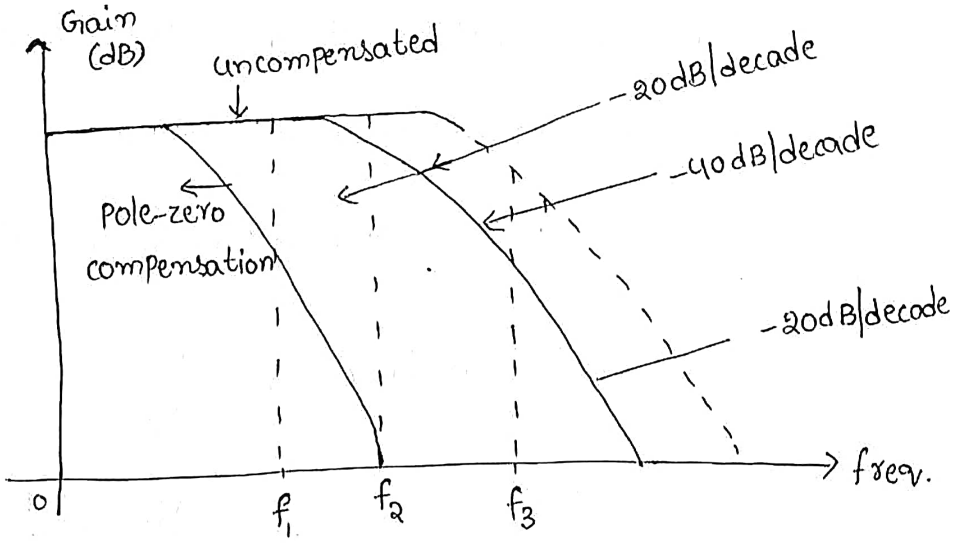
But $$A = \frac{A_{OL}}{\left[1+j\left(\frac{f}{f_1}\right)\right]\left[1+j\left(\frac{f}{f_2}\right)\right]\left[1+j\left(\frac{f}{f_3}\right)\right]}$$

$$\Rightarrow A' = \left[\frac{1+j\left(\frac{f}{f_1}\right)}{1+j\left(\frac{f}{f_0}\right)}\right] \cdot \frac{A_{OL}}{\left[1+j\left(\frac{f}{f_1}\right)\right]\left[1+j\left(\frac{f}{f_2}\right)\right]\left[1+j\left(\frac{f}{f_3}\right)\right]}$$

$$\Rightarrow \boxed{A' = \frac{A_{OL}}{\left[1+j\left(\frac{f}{f_0}\right)\right]\left[1+j\left(\frac{f}{f_2}\right)\right]\left[1+j\left(\frac{f}{f_3}\right)\right]}} \quad ; 0 < f_0 < f_1 < f_2 < f_3$$

The 1st corner frequency is f_0 and gain starts rolling off at -20 dB/decade at f_0.

→ At $f = f_1$, there is pole-zero cancellation and rolling rate continues at -20 dB/decade.



Advantage

→ Band width is more as compared to Dominant Pole compensation.

Internal compensation technique :-

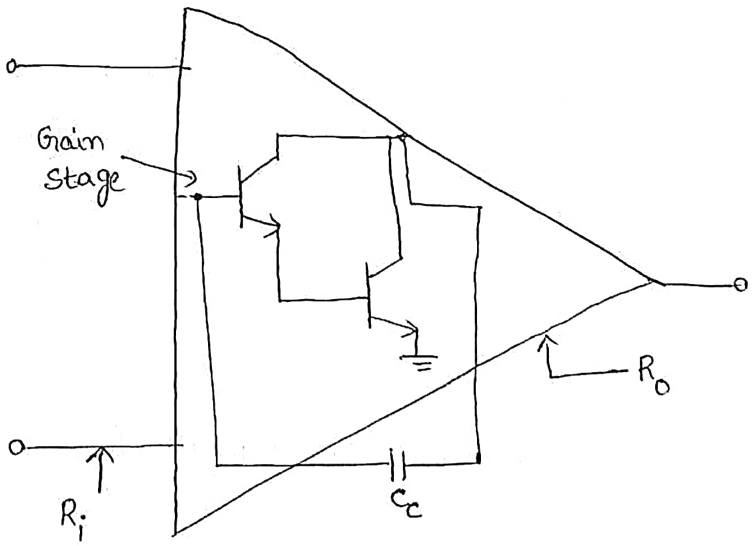
In OP-amps IC 741, compensation is provided Internally, which is generally built in lag compensation.

→ A capacitor ranging from 10 to 30PF is fabricated between Input and output stage to achieve compensation. This type of compensation is called "miller effect compensation" such OP-amps are called compensated OP-amps.

miller effect compensation :-

The main drack back in dominant pole compensation is the reduction in band width. In dominant pole compensation, capacitor is connected to ground from output terminal.

In miller effect compensation capacitor is connected in feed back path.



The Gain of the darling ton stage is given by

$$a_2 = -G_{mc} R_o$$

G_{mc} → Transconductance of the stage

$$z_{cm} = \frac{z_{cc}}{1+a_2}$$

where, $Z_{cm} = \frac{1}{j\omega C_m}$, $Z_{cc} = \frac{1}{j\omega C_c}$

$$\Rightarrow \frac{1}{j\omega C_m} = \frac{\frac{1}{j\omega C_c}}{1+a_2}$$

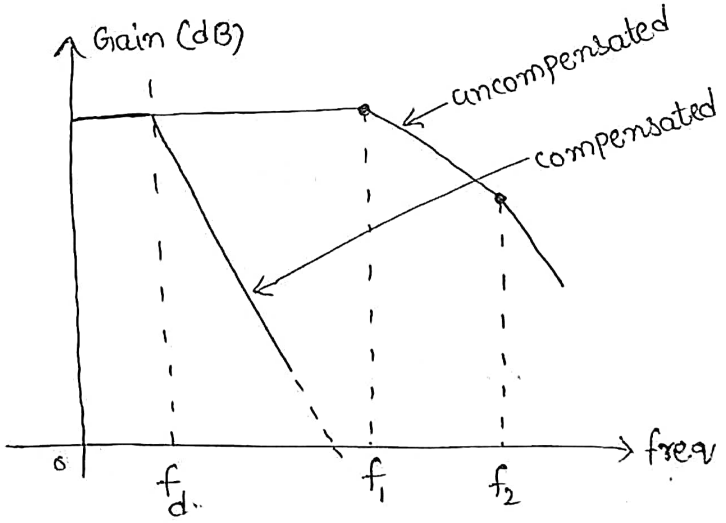
$$\Rightarrow \frac{(1+a_2)}{j\omega C_c} = \frac{1}{j\omega C_m} \Rightarrow \frac{1}{j\omega C_m} = \frac{1}{(1+a_2) j\omega C_c}$$

$$\Rightarrow \boxed{C_m = (1+a_2) C_c}$$

The miller equivalent capacitance C_m forms a low pass RC section with input R_i, whose corner frequency is given by

$$\boxed{f_d = \frac{1}{2\pi C_m R_i}}$$

The uncompensated and compensated magnitude plots are shown in fig.



Advantage :-

→ It Increases the band width.

3. Linear and Non-linear Applications of op-amp

Introduction:-

1. **Linear circuit:-** The output voltage varies linearly with respect to Input voltage. * feed back is used from output to Inverting termina

→ Applications are Adder, Subtractor, Integrator, differentiator, buffer etc..

2. **Non-linear circuit:-**

→ Feed back is used from output to the Non inverting input terminal.

→ The feed back may be provided to Inverting input terminal using non linear elements like diodes, transistors etc..

→ Applications are comparators, Schmitt trigger, Log amplifier, Antilog Amplifier, Precision rectifier.

Virtual ground :-

This means the differential Input voltage V_d between the Inverting and Non Inverting Input terminals is zero

i.e $V_d = V_A - V_B$

$0 = V_A - V_B \Rightarrow \boxed{V_A = V_B}$

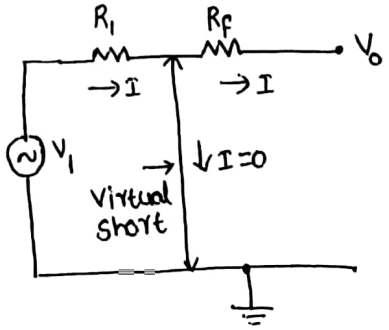


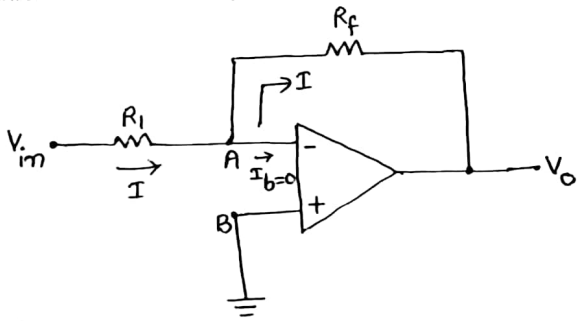
Fig:- concept of Virtual ground

For ex,

If the Non-Inverting terminal is grounded, according to the concept of virtual short, Inverting terminal is also at ground potential, there is no physical connection between Inverting terminal and ground. This is the principle of virtual ground.

Ideal Inverting Amplifier :-

An Amplifier which provides a phase shift of 180° between Input and output is called Inverting Amplifier.



From fig,

$V_B = 0$

concept of virtual ground, $V_A = 0$

Input side, $I = \frac{V_{in} - V_A}{R_1}$

$= \frac{V_{in} - 0}{R_1} = \frac{V_{in}}{R_1}$ — ①

output side, $I = \frac{V_A - V_o}{R_f} = \frac{0 - V_o}{R_f}$

$= \frac{-V_o}{R_f}$ — ②

equating eq ①, ②

$\frac{V_{in}}{R_1} = \frac{-V_o}{R_f} \Rightarrow V_o = \frac{-R_f}{R_1} V_{in}$

$$\Rightarrow \frac{V_o}{V_{in}} = -\frac{R_f}{R_1}$$

$$\Rightarrow \boxed{A_{V_f} = -\frac{R_f}{R_1}}$$ where A_{V_f} → Gain with feed back

'−' sign Indicates that Polarity of output is opposite to Input.

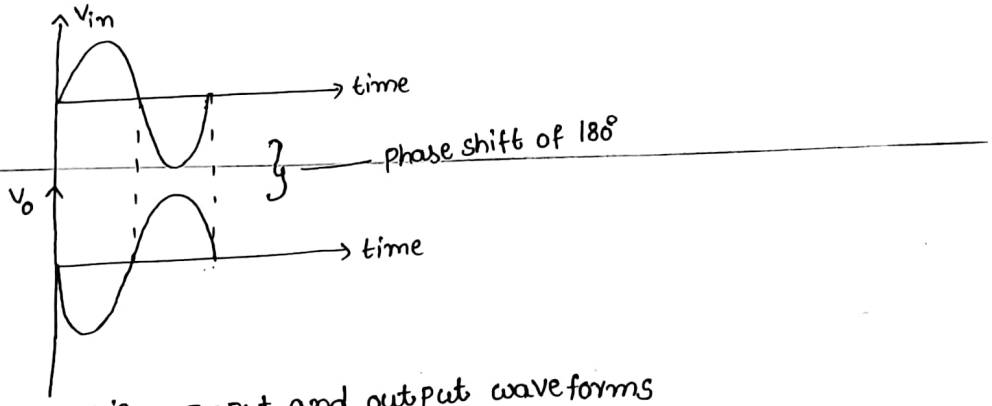
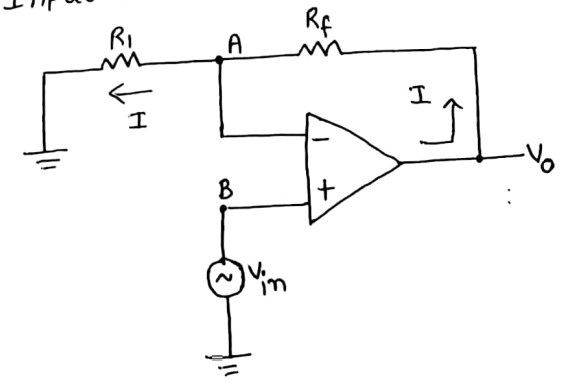


Fig:- Input and output waveforms

Ideal Non-Inverting Amplifier :-

An Amplifier which Amplifies the Input with out producing any phase shift between Input and output is called Non-Inverting Amplifier.



From fig,

$V_B = V_{in}$

concept of virtual ground, $V_A = V_{in}$

output side, $I = \frac{V_o - V_A}{R_f} = \frac{V_o - V_{in}}{R_f}$ —①

At Inverting terminal,

$$I = \frac{V_A - 0}{R_1} = \frac{V_A}{R_1} = \frac{V_{in}}{R_1} \quad \text{—②}$$

equating eq①, ②

$$\Rightarrow \frac{V_o - V_{in}}{R_f} = \frac{V_{in}}{R_1}$$

$$\Rightarrow \frac{V_o}{R_f} - \frac{V_{in}}{R_f} = \frac{V_{in}}{R_1}$$

$$\Rightarrow \frac{V_o}{R_f} = \frac{V_{in}}{R_1} + \frac{V_{in}}{R_f}$$

$$= V_{in}\left[\frac{1}{R_1} + \frac{1}{R_f}\right] \Rightarrow V_{in}\left[\frac{R_f + R_1}{R_1 R_f}\right]$$

$$\Rightarrow \frac{V_o}{R_f} = V_{in}\left[\frac{R_f + R_1}{R_1 R_f}\right]$$

$$\Rightarrow V_o = V_{in} \cdot R_f \left[\frac{R_f + R_1}{R_1 R_f}\right]$$

$$\Rightarrow \frac{V_o}{V_{in}} = \frac{R_f}{R_1} + \frac{R_1}{R_1}$$

$$\Rightarrow \boxed{A_{VF} = 1 + \frac{R_f}{R_1}}$$

The '+' sign Indicates there is no phase shift between Input and output.

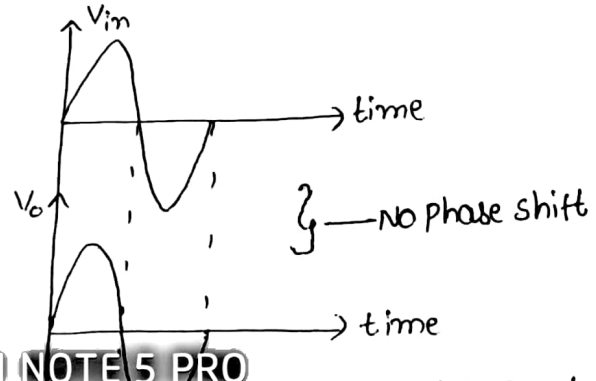


Fig:- Input and output waveforms

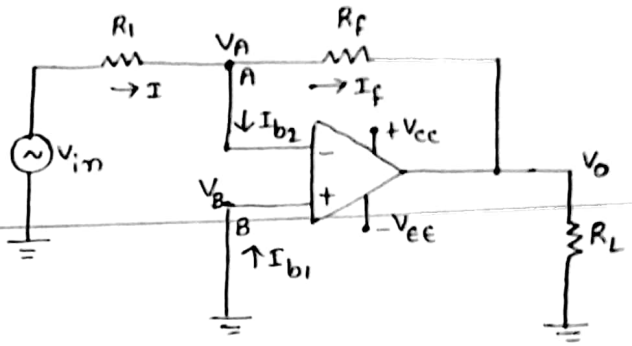
Practical Inverting Amplifier :-

The practical Inverting op-Amp has major differences as compared to ideal, they are

i) Input resistance R_i is less than ∞, hence Input current is finite

ii) A_{OL} is less than ∞

iii) R_o is not zero.



Apply KCL, at node 'A'

$$I = I_{b_2} + I_f$$

I_{b_2} can be neglected, since it flows to Inverting terminal

$$\Rightarrow I \approx I_f \quad \text{—①}$$

$$\Rightarrow \frac{V_{in} - V_A}{R_1} = \frac{V_A - V_o}{R_f} \quad \text{— ②}$$

W.K.T $V_o = A_{OL} V_d$

$$= A_{OL}(V_1 - V_2) \quad = A_{OL}(V_B - V_A)$$

From fig, Input is inverting (-) so non Inverting Input $V_B = 0$

$$\Rightarrow V_o = A_{OL}(0 - V_A) \quad \Rightarrow V_o = -V_A \cdot A_{OL}$$

$$\Rightarrow V_A = \frac{-V_o}{A_{OL}} \quad \text{—③}$$

sub. eq ③ in ②

$$\frac{V_{in} + \frac{V_o}{A_{OL}}}{R_1} = \frac{\frac{-V_o}{A_{OL}} - V_o}{R_f}$$

$$\Rightarrow \left(V_{in} + \frac{V_o}{A_{OL}}\right) R_f = \left(\frac{-V_o}{A_{OL}} - V_o\right) R_1$$

$$\Rightarrow V_{in} R_f + \frac{V_o}{A_{OL}} R_f = \frac{-V_o}{A_{OL}} R_1 - V_o R_1$$

$$\Rightarrow V_{in} R_f = \frac{-V_o}{A_{OL}} R_f - \frac{V_o}{A_{OL}} R_1 - V_o R_1$$

$$= -V_o \left[\frac{R_f}{A_{OL}} + \frac{R_1}{A_{OL}} + R_1\right]$$

$$= -V_o \left[\frac{R_f + R_1 + A_{OL} R_1}{A_{OL}}\right]$$

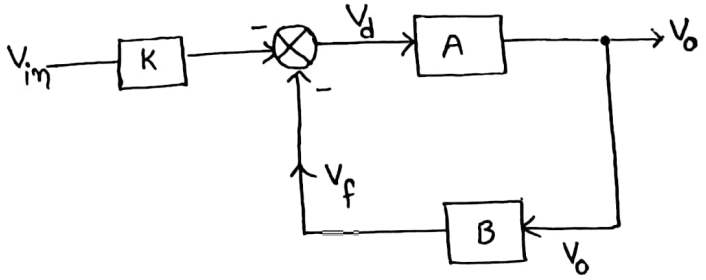
$$\Rightarrow V_o = \frac{-V_{in} R_f}{R_f + R_1 + A_{OL} R_1} \cdot A_{OL}$$

$$A_{CL} \Rightarrow \frac{V_o}{V_{in}} = \frac{-A_{OL} R_f}{R_1 + R_f + A_{OL} R_1} \quad \text{—— (4)}$$

Ideally, A_{OL} is very large, $A_{OL} R_1 >> R_1 + R_f$ hence $R_1 + R_f$ is neglected.

$$\Rightarrow A_{CL} = \frac{-A_{OL} R_f}{A_{OL} R_1} \Rightarrow \boxed{A_{CL} = \frac{-R_f}{R_1} \text{ (ideal)}}$$

Block diagram of Practical Inverting Amplifier :-



From fig,

$$V_d = -V_{in} k - V_f \quad \text{—— (1)}$$

$$V_o = V_d A \quad \text{—— (2)}$$

$V_f = \beta V_o$ —— (3)

Sub. eq① in ②

$$V_o = (-V_{in}k - V_f)A \quad \text{— ④}$$

Sub. eq ③ in ④

$$V_o = (-V_{in}k - BV_o)A \quad \text{— ⑤}$$

$$V_o = -V_{in}kA - BV_oA$$

$$\Rightarrow V_o + BV_oA = -V_{in}kA$$

$$\Rightarrow V_o(1+BA) = -V_{in}kA$$

$$\Rightarrow \frac{V_o}{V_{in}} = \frac{-kA}{1+BA} \quad \text{— ⑥}$$

From eq ⑥ in previous topic, $A_{CL} = \frac{-A_{OL}R_f}{R_1+R_f+A_{OL}R_1}$ — ⑦

Divide (R_1+R_f) Numerator & Denominator term

$$A_{CL} = \frac{\frac{-A_{OL}R_f}{R_1+R_f}}{\frac{R_1+R_f+A_{OL}R_1}{R_1+R_f}} = \frac{\frac{-A_{OL}R_f}{R_1+R_f}}{1+\frac{A_{OL}R_1}{R_1+R_f}} \quad \text{— ⑧}$$

compare eq ⑥, ⑧ we get,

$$A = A_{OL},\ k = \frac{R_f}{R_1+R_f},\ B = \frac{R_1}{R_1+R_f}$$

$$\Rightarrow \boxed{A_{CL} = \frac{-Ak}{1+BA}} \quad \text{— ⑨}$$

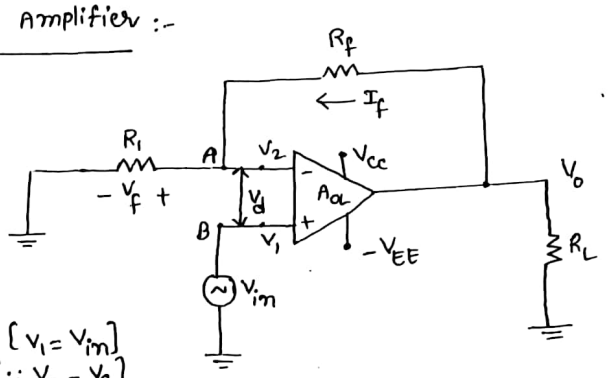
Ideally, $BA >> 1 \approx 1+BA = BA$

$$\Rightarrow A_{CL} = \frac{-Ak}{BA} = \frac{-k}{B}$$

$$= -\frac{R_f}{R_1+R_f} \times \frac{R_1+R_f}{R_1} \Rightarrow \boxed{A_{CL} = -\frac{R_f}{R_1}}$$

Practical Non-Inverting Amplifier :-

$R_f \rightarrow$ feed back resistor



From fig.

$$V_d = (V_1 - V_2) A_{OL}$$

$$V_o = (V_{in} - V_f) A_{OL} \quad [V_1 = V_{in}] \quad [\because V_2 = V_f] \quad \text{— ①}$$

Apply voltage divider rule,

$$V_f = \frac{R_1}{R_1 + R_f} \cdot V_o \quad \text{— ②}$$

sub. eq ② in eq ①

$$V_o = \left(V_{in} - \frac{R_1 V_o}{R_1 + R_f}\right) A_{OL}$$

$$\Rightarrow V_o = A_{OL} V_{in} - A_{OL} \frac{V_o R_1}{R_1 + R_f}$$

$$\Rightarrow V_o + A_{OL} \frac{V_o R_1}{R_1 + R_f} = A_{OL} V_{in}$$

$$\Rightarrow V_o \left[1 + A_{OL} \frac{R_1}{R_1 + R_f}\right] = A_{OL} V_{in}$$

$$\Rightarrow V_o = \frac{A_{OL}}{1 + A_{OL} \frac{R_1}{R_1 + R_f}} \cdot V_{in}$$

$$\Rightarrow \frac{V_o}{V_{in}} = \frac{A_{OL}}{\frac{R_1 + R_f + A_{OL} R_1}{R_1 + R_f}}$$

$$\Rightarrow \boxed{A_{CL} = \frac{A_{OL}(R_1 + R_f)}{R_1 + R_f + A_{OL} R_1}} \quad \text{— ③}$$

consider,

$A_{OL}R_1 >> (R_1+R_f)$

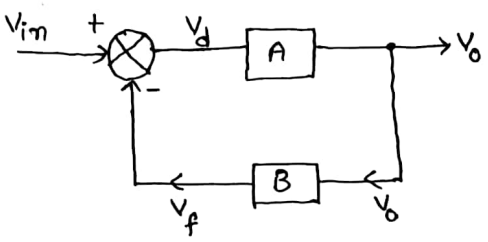
then eqv ③ changes to, $A_{CL} = \frac{A_{OL}(R_1+R_f)}{A_{OL}R_1}$

$\Rightarrow A_{CL} = \frac{R_1+R_f}{R_1}$

$\Rightarrow \boxed{A_{CL} = 1+\frac{R_f}{R_1} \text{ (ideal)}}$

Block diagram of Practical Non-Inverting Amplifier :-

Forward Path gain 'A' and feed back path gain 'B'.



From fig.

$V_d = V_{in} - V_f$ — ①

$V_o = AV_d$ — ②

$V_f = BV_o$ — ③

sub. eqv ① in eqv ②

$V_o = A(V_{in} - V_f)$ — ④

sub. eqv ③ in eqv ④

$V_o = A(V_{in} - BV_o)$

$\Rightarrow V_o = AV_{in} - BV_oA$

$\Rightarrow V_o + BV_oA = AV_{in}$

$\Rightarrow V_o(1+BA) = AV_{in}$

$\Rightarrow \frac{V_o}{V_{in}} = \frac{A}{1+BA}$ — ⑤

w.k.t $A_{CL} = \frac{A_{OL}(R_1+R_f)}{R_1+R_f+R_1A_{OL}}$

Divide N.r and D.r by (R_1+R_f)

$$\Rightarrow A_{CL} = \frac{\frac{A_{OL}(R_1+R_f)}{R_1+R_f}}{\frac{R_1+R_f+R_1A_{OL}}{R_1+R_f}}$$

$$\Rightarrow A_{CL} = \frac{A_{OL}}{1+A_{OL}\left(\frac{R_1}{R_1+R_f}\right)} \quad \text{— (6)}$$

compare eq (5) and eq (6), we get

$$A = A_{OL},\ B = \frac{R_1}{R_1+R_f}$$

$$\Rightarrow A_{CL} = \frac{A}{1+BA}$$

consider $1+BA \approx BA$

$$\Rightarrow A_{CL} = \frac{A}{BA} = \frac{1}{B}$$

$$= \frac{1}{\frac{R_1}{R_1+R_f}} = \frac{R_1+R_f}{R_1}$$

$$\Rightarrow \boxed{A_{CL} = 1+\frac{R_f}{R_1}}$$

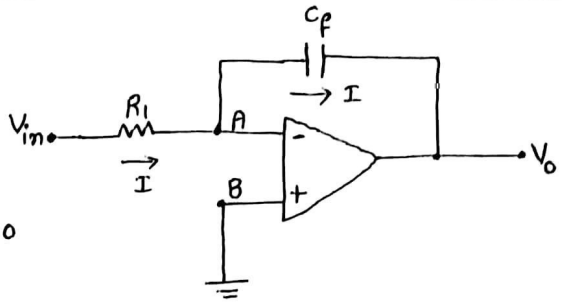
Integrator :-

The output voltage is the Integration of the Input voltage.

→ The Integrator circuit can be obtained without using active devices like op-amp, transistors the Integrator called as "Passive Integrator".

→ Integrator using an Active devices like op-amp is called "Active Integrator".

Ideal Active Integrator :-



From fig, $V_B = 0$

concept of virtual ground, $V_A = 0$

Input side, $I = \frac{V_{in} - V_A}{R_1} = \frac{V_{in} - 0}{R_1}$

$= \frac{V_{in}}{R_1}$ —①

output side, $I = C_f \frac{d}{dt}(V_A - V_o)$

$= C_f \frac{d}{dt}(0 - V_o) = -C_f \frac{dV_o}{dt}$ —②

equating eq ①, ②

$\Rightarrow \frac{V_{in}}{R_1} = -C_f \frac{dV_o}{dt}$ —③

Integrating eq ③ on both sides,

$\Rightarrow \int_0^t \frac{V_{in}}{R_1} dt = -C_f \int \frac{dV_o}{dt} dt$

$= -C_f V_o$

$\Rightarrow \boxed{V_o = \frac{-1}{R_1 C_f} \int_0^t V_{in}\, dt}$ —④

$R_1 C_f \rightarrow$ Time constant

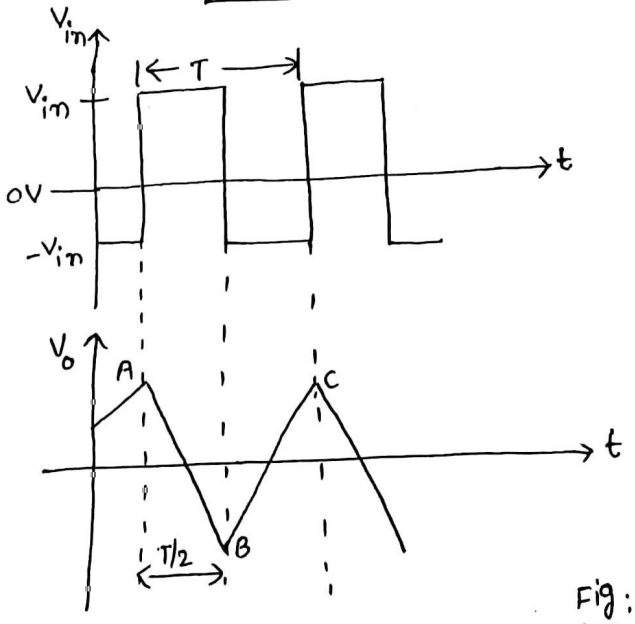


Fig :- Input and output wavefor

Frequency response of Ideal Integrator :-

w.k.T $V_0(t) = -\frac{1}{R_1 C_f} \int_0^t V_{in}\, dt$

Taking Laplace transform,

$$V_0(s) = -\frac{1}{sR_1C_f} V_{in}(s)$$

Let $s = j\omega$,

$$\Rightarrow V_0(j\omega) = \frac{-1}{j\omega R_1 C_f} V_{in}(j\omega)$$

$$\Rightarrow \frac{V_0(j\omega)}{V_{in}(j\omega)} = -\frac{1}{j\omega R_1 C_f} \quad -(5)$$

The magnitude value is, $A = \left|\frac{V_0(j\omega)}{V_{in}(j\omega)}\right| = \left|-\frac{1}{j\omega R_1 C_f}\right|$

$$\Rightarrow A = \frac{1}{\omega R_1 C_f} = \frac{1}{2\pi f R_1 C_f} \quad -(6) \qquad \Rightarrow A = \frac{f_b}{f} \quad -(7) \quad \left[\because f_b = \frac{1}{2\pi R_1}\right.$$

Let $f = 0$, eq (6) becomes $A = \infty$

and $f = f_b \Rightarrow A = 1$ i.e 0 dB.

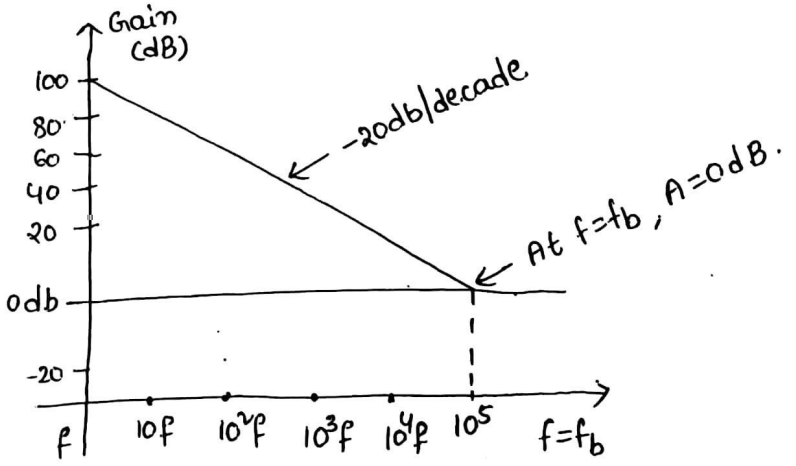


Fig :- frequency response of Ideal Integrator.

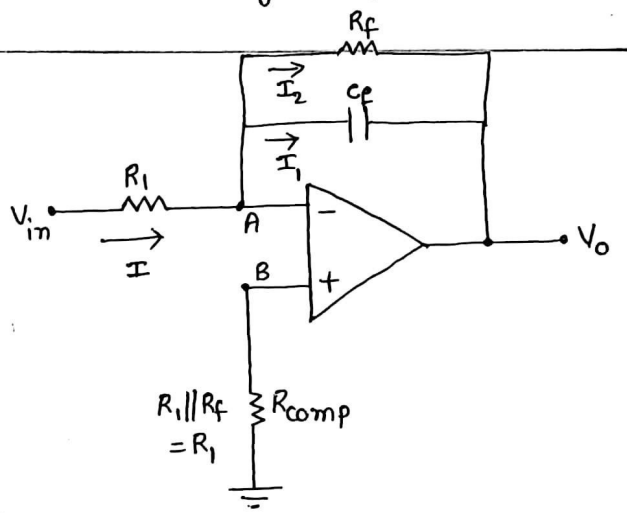
The gain rolls off at a rate of -20dB/decade.

Errors in an Ideal Integrator :-

→ In the presence of Input signal, offset voltage and bias current contribute an error voltage at the output. It is not possible to get a true Integration of Input signal at the output. output wave form may be distorted due to error voltage.

→ Another limitation is Band width is very small. hence ideal Integrator used for very small frequency range of Input only.

practical Integrator :-



From fig,

$V_B = 0 \Rightarrow V_A = 0$

Apply KCL at node 'A'

$$I = I_1 + I_2 \quad \text{—①}$$

From fig, $I = \frac{V_{in} - V_A}{R_1} = \frac{V_{in} - 0}{R_1}$

$$= \frac{V_{in}}{R_1} \quad \text{—②}$$

and $I_1 = C_f \frac{d}{dt}(V_A - V_o) = C_f \frac{d}{dt}(0 - V_o)$

$$= -C_f \frac{dV_o}{dt} \quad \text{—③}$$

and $I_2 = \frac{V_A - V_o}{R_f} = \frac{0 - V_o}{R_f} = \frac{-V_o}{R_f}$ —④

sub. eq②, ③, ④ in eq①

$$\Rightarrow \frac{V_{in}}{R_1} = -C_f \frac{dV_o}{dt} - \frac{V_o}{R_f}$$

Apply Laplace transform,

$$\frac{V_{in}(s)}{R_1} = -s C_f V_o(s) - \frac{V_o(s)}{R_f} \quad \text{— (5)}$$

$$= -V_o(s)\left[s C_f + \frac{1}{R_f}\right]$$

$$= -V_o(s)\left[\frac{R_f s C_f + 1}{R_f}\right]$$

$$\Rightarrow V_o(s) = \frac{-R_f}{R_1(R_f s C_f + 1)} \cdot V_{in}(s) \quad \text{— (6)}$$

$$= \frac{\frac{-1}{s C_f R_f R_1 + R_1}}{R_f} \cdot V_{in}(s)$$

$$= -\frac{1}{s C_f R_1 + \left(\frac{R_1}{R_f}\right)} \cdot V_{in}(s)$$

when R_f is large value, R_1/R_f can be neglected, hence

$$V_o(s) = -\frac{1}{s C_f R_1} V_{in}(s)$$

Apply Inverse Laplace transform,

$$\boxed{V_o(t) = -\frac{1}{R_1 C_f} \int V_{in}(t)\, dt}$$

Frequency response of practical Integrator :-

from eq (6), $$\frac{V_o(s)}{V_{in}(s)} = -\frac{R_f/R_1}{1 + s R_f C_f}$$

put $s \to j\omega$

then, $$\frac{V_o(j\omega)}{V_{in}(j\omega)} = -\frac{R_f/R_1}{1 + j\omega R_f C_f}$$

$$\Rightarrow A = -\frac{R_f/R_1}{1 + j 2\pi f R_f C_f}$$

$$\Rightarrow A = -\frac{R_f/R_1}{1+j\,f/f_a} \qquad \left[\because f_a = \frac{1}{2\pi R_f C_f}\right]$$

magnitude, $|A| = \left|-\frac{R_f/R_1}{1+j(f/f_a)}\right|$

$$= \frac{R_f/R_1}{\sqrt{1+(f/f_a)^2}} \quad \text{— (1)}$$

Let $f = 0 \rightarrow |A| = R_f/R_1$

$$= 20\log\left(\frac{R_f}{R_1}\right) dB$$

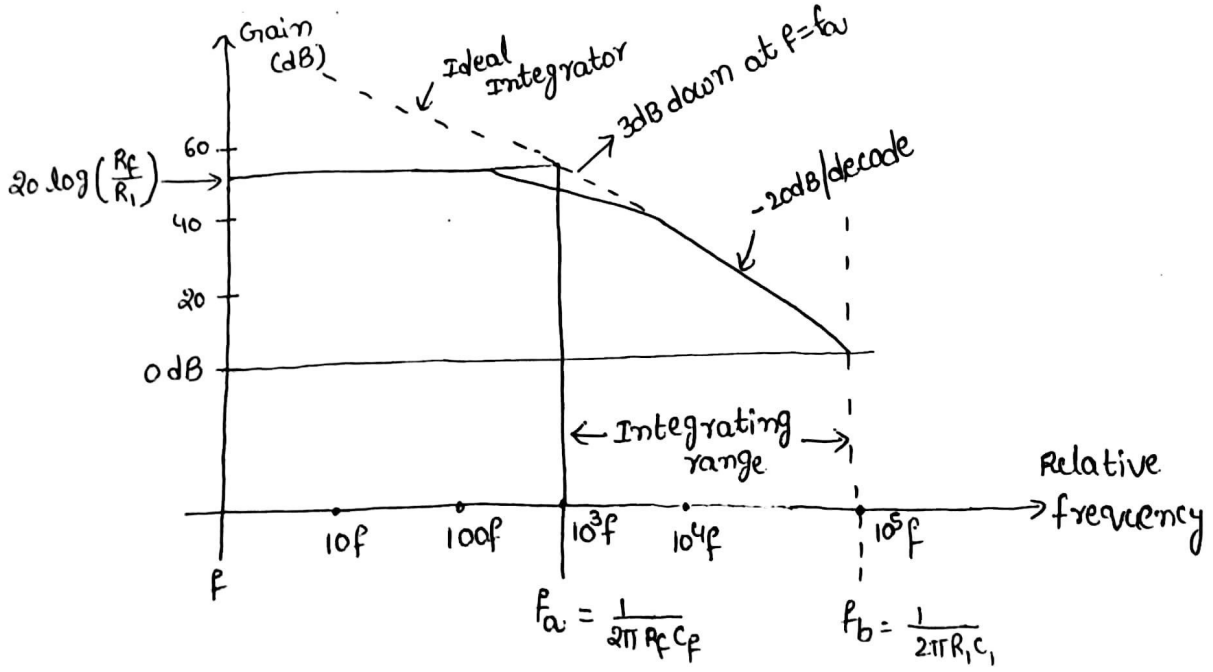
Let $f = f_a \rightarrow |A| = \frac{R_f/R_1}{\sqrt{1+1}} = \frac{R_f/R_1}{\sqrt{2}} = 0.707\,\frac{R_f}{R_1}$

i.e $20\log|A| = 20\log\left(0.707\,\frac{R_f}{R_1}\right)$

$$= 20\log(0.707) + 20\log\left(\frac{R_f}{R_1}\right)$$

$$= -3dB + \text{D.C gain}$$

→ At $f = f_a$, magnitude of gain drops by 3dB frequency. which is the break frequency.



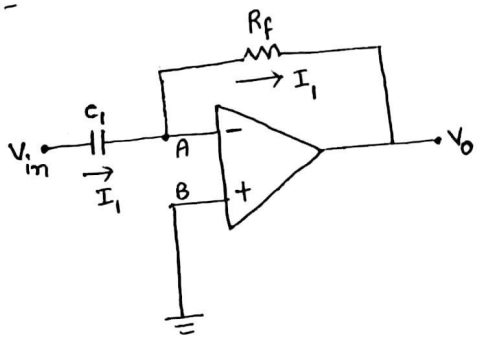
Applications of Practical Integrator :-

→ Analog computers
→ Analog to digital converters
→ Various signal wave shaping circuits
→ Ramp generators

Differentiator :-

The circuit which produces the output voltage is the differentiation of Input voltage is called differentiator.

Ideal Active op-amp differentiator :-



From fig, $V_B = 0$

concept of virtual ground

$V_A = 0$

Input side, $I_1 = C_1 \frac{d}{dt}(V_{in} - V_A)$

$= C_1 \frac{d}{dt}(V_{in} - 0)$

$= C_1 \frac{d}{dt} V_{in}$ —①

output side, $I_1 = \frac{V_A - V_o}{R_f} = \frac{0 - V_o}{R_f} = \frac{-V_o}{R_f}$ —②

equating eq①, ②

$C_1 \frac{dV_{in}}{dt} = \frac{-V_o}{R_f}$

$\Rightarrow \boxed{V_o = -C_1 R_f \frac{dV_{in}}{dt}}$ —③

where $C_1 R_f$ → Time cons

This equation shows that output is $C_1 R_f$ times the differentiation of Input.

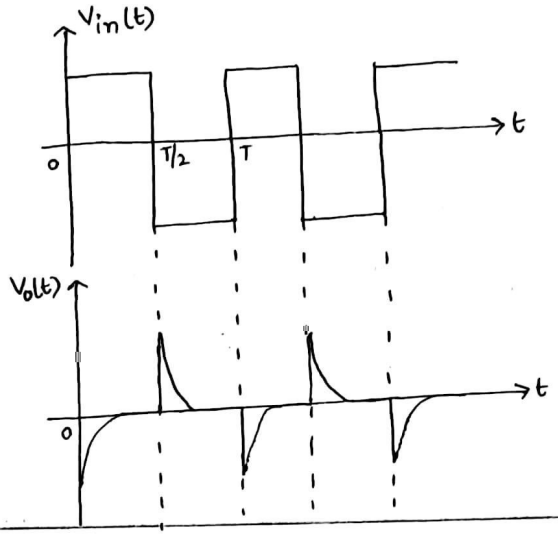


Fig :- Input and output for square wave input

Frequency response of ideal differentiator :-

$$\text{w.k.T} \quad V_0(t) = -R_f C_1 \frac{dV_{in}}{dt}$$

Taking Laplace transform,

$$V_0(s) = -sR_f C_1 V_{in}(s)$$

Put $s = j\omega$

$$V_0(j\omega) = -j\omega R_f C_1 V_{in}(j\omega)$$

$$\Rightarrow \frac{V_0(j\omega)}{V_{in}(j\omega)} = -j\omega R_f C_1$$

magnitude is,

$$A = \left| \frac{V_0(j\omega)}{V_{in}(j\omega)} \right| = \left| -j\omega R_f C_1 \right|$$

$$A = \omega R_f C_1 = 2\pi f R_f C_1 \quad \text{—— (9)}$$

At $f=0$, $A=0$

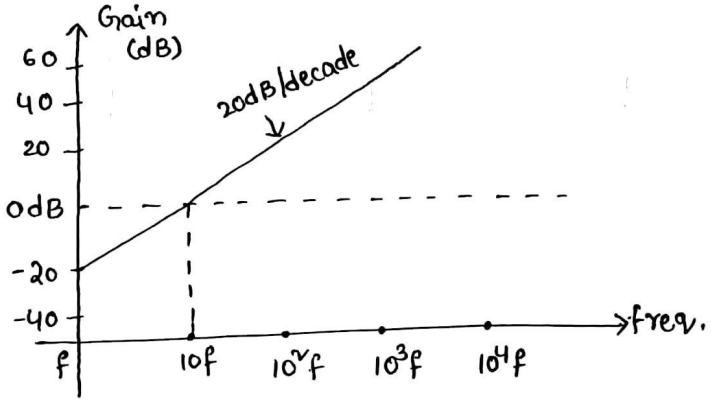
From eq ④, As the frequency increases, gain also Increases.

From eq ④, consider $f_a = \frac{1}{2\pi R_f C_1}$

then eq ④ changes to $A = f/f_a$ —⑤

At $f=f_a$, then $A=1$ (or) $20\log 1 = 0dB$. it gives increase in gain is at a rate of 20 dB/decade.

The frequency response of such Ideal differentiator as shown in fig.



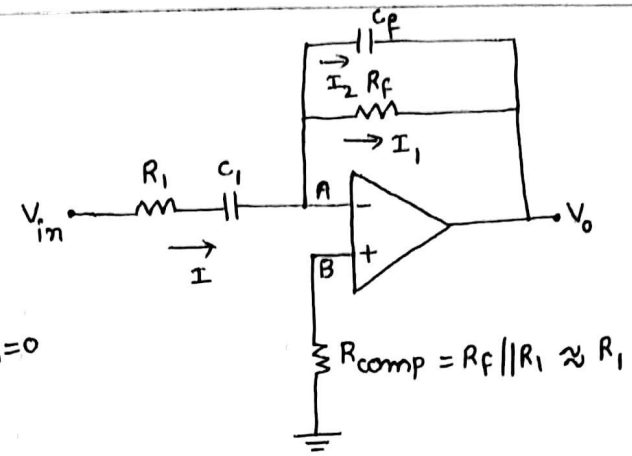
Disadvantages of an ideal differentiator :-

→ Gain Increases as frequency increases, At some high frequency the differentiator may become unstable and break into oscillations. There is a possibility that op-amp go into saturation.

→ At high frequencies, differentiator circuit suffers from its stability and noise problems.

→ These problems can be corrected by using practical differentia circuit.

practical differentiator :-



From fig,

$V_B = 0$.

concept of virtual ground $V_A = 0$

From the circuit,

$$I = \frac{V_{in} - V_A}{Z_1} = \frac{V_{in} - 0}{Z_1} = \frac{V_{in}(s)}{Z_1} \quad \text{—①}$$

where, $Z_1 = R_1 + C_1$

Apply Laplace, then

$$Z_1 = R_1 + \frac{1}{sC_1}$$

$$= \frac{sC_1 R_1 + 1}{sC_1} \quad \text{—②}$$

Sub. eq② in ①

$$\Rightarrow I = \frac{V_{in}(s)}{\frac{sC_1R_1 + 1}{sC_1}} = \frac{sC_1 V_{in}(s)}{sC_1R_1 + 1} \quad \text{—③}$$

Now $I_1 = \frac{V_A - V_o}{R_f} = \frac{0 - V_o}{R_f} = -\frac{V_o}{R_f} \Rightarrow \frac{-V_o(s)}{R_f}$ —④ [∵ L.T.

$$I_2 = C_f \frac{d}{dt}(V_A - V_o)$$

$$= C_f \frac{d}{dt}(0 - V_o) = -C_f \frac{dV_o}{dt}$$

$$= -sC_f V_o(s) \quad \text{—⑤}$$

Apply KCL at node 'A'

$$I = I_1 + I_2 \quad \text{—⑥}$$

sub. eq ③, ④, ⑤ in eq ⑥,

$$\frac{sC_1 V_{in}(s)}{1+sR_1C_1} = \frac{-V_o(s)}{R_f} - sC_f V_o(s)$$

$$= \frac{-V_o(s) - R_f s C_f V_o(s)}{R_f}$$

$$= -V_o(s)\left[\frac{1+sR_fC_f}{R_f}\right]$$

$$\Rightarrow V_o(s) = \frac{-sR_fC_1 V_{in}(s)}{(1+sR_fC_f)(1+sR_1C_1)} \quad \text{—— ⑦}$$

If $R_fC_f = R_1C_1$ then eq ⑦ changes to

$$V_o(s) = \frac{-sR_fC_1 V_{in}(s)}{(1+sR_fC_f)^2} \quad \text{—— ⑧}$$

If $R_fC_1 >> R_1C_1$ (or) R_fC_f

$$\Rightarrow V_o(s) = -sR_fC_1 V_{in}(s)$$

Apply Inverse Laplace,

$$\Rightarrow \boxed{V_o(t) = -R_fC_1 \frac{dV_{in}(t)}{dt}} \quad \text{—— ⑨} \qquad \left[\because s = \frac{d}{dt}\right]$$

From eq ⑨, output voltage is the R_fC_1 times the differentiation of the input.

Frequency response of practical differentiator :-

From eq (8), $$\frac{V_o(s)}{V_{in}(s)} = \frac{-sR_fC_1}{(1+sR_1C_1)^2}$$

Put $s = j\omega$

$$\frac{V_o(j\omega)}{V_{in}(j\omega)} = \frac{-j\omega R_f C_1}{(1+j\omega R_1 C_1)^2}$$

$$= \frac{-j2\pi f R_f C_1}{(1+j2\pi f R_1 C_1)^2} \quad \text{— (10)}$$

Let $f_b = \frac{1}{2\pi R_1 C_1}$ and $f_a = \frac{1}{2\pi R_f C_1}$

then eq (10) becomes,

$$\frac{V_o(j\omega)}{V_{in}(j\omega)} = \frac{-j(f/f_a)}{1+j(f/f_b)^2} \quad \text{— (11)}$$

magnitude, $$A = \left|\frac{V_o(j\omega)}{V_{in}(j\omega)}\right| = \frac{f/f_a}{\left[\sqrt{1+(f/f_b)^2}\right]^2}$$

$$\Rightarrow \boxed{A = \frac{f/f_a}{1+(f/f_b)^2}}$$

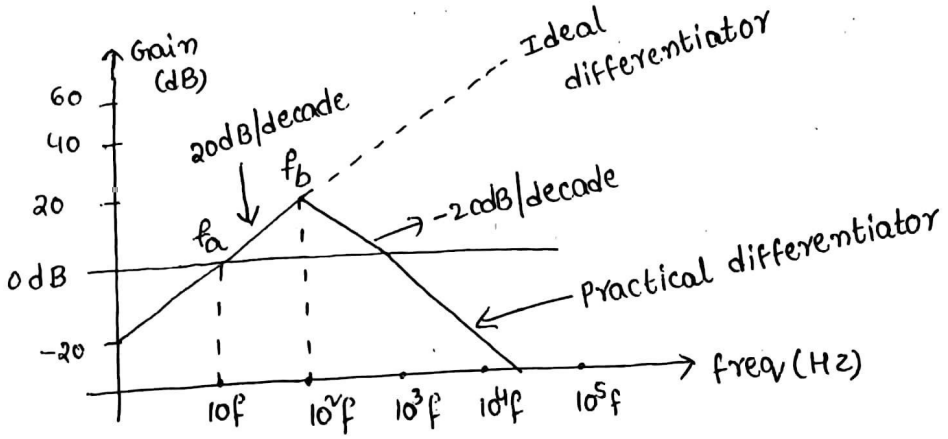


Fig :- frequency response of practical differentiator

From fig,

frequency Increases, gain Increases till $f=f_b$ at 20dB/decade after $f=f_b$ the gain becomes decreases at 20 dB/decade.

Applications of practical differentiator :-

→ wave shaping circuits
→ Rate of change detector in FM demodulators.
→ Avoided in Analog computers.

Summer (or) Adder circuit :-

The output voltage gives addition of applied input voltages.

→ Depending upon the sign of the output, summer circuit divided into Inverting summer and Non-Inverting summer.

1. Inverting summer :-

In this circuit Input signals (V_1, V_2) are applied to Inverting terminal.

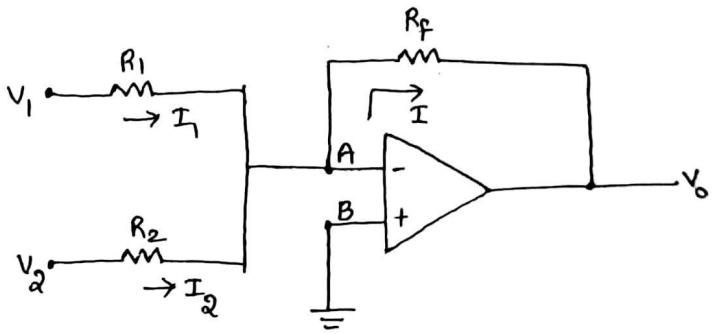


Fig:- Inverting summer

From fig. $V_B = 0$

concept of virtual ground, $V_A = 0$

Input side, $I_1 = \frac{V_1 - V_A}{R_1} = \frac{V_1 - 0}{R_1} = \frac{V_1}{R_1}$ —①

$I_2 = \frac{V_2 - V_A}{R_2} = \frac{V_2 - 0}{R_2} = \frac{V_2}{R_2}$ —②

output side, $I = \frac{V_A - V_0}{R_f} = \frac{0 - V_0}{R_f} = \frac{-V_0}{R_f}$ —③

Apply KCL at node 'A'

$I = I_1 + I_2$ —④

sub. eqn ①, ②, ③ in ④

$$\frac{V_1}{R_1} + \frac{V_2}{R_2} = \frac{-V_0}{R_f}$$

$$\Rightarrow V_0 = -R_f\left[\frac{V_1}{R_1} + \frac{V_2}{R_2}\right] \quad —⑤$$

If $R_f = R_1 = R_2$:

$$\Rightarrow \boxed{V_0 = -(V_1 + V_2)}$$

'–' Indicates phase difference between Input & output

2. Non-Inverting summing Amplifier :-

In this circuit we are applying Input Voltages to non-Inverting terminal.

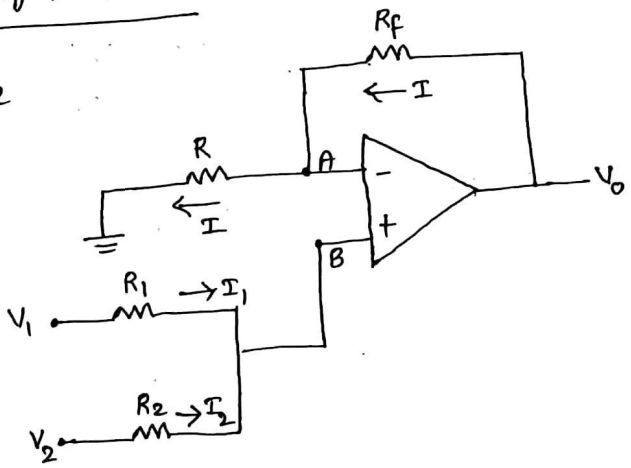


Fig :- Non-Inverting summer

Input side,

$$I_1 = \frac{V_1 - V_B}{R_1} \quad \text{and} \quad I_2 = \frac{V_2 - V_B}{R_2}$$

Input current of OP-Amp zero i.e

$$I_1 + I_2 = 0$$

$$\frac{V_1 - V_B}{R_1} + \frac{V_2 - V_B}{R_2} = 0$$

$$\Rightarrow \frac{V_1}{R_1} - \frac{V_B}{R_1} + \frac{V_2}{R_2} - \frac{V_B}{R_2} = 0$$

$$\Rightarrow \frac{V_1}{R_1} + \frac{V_2}{R_2} = \frac{V_B}{R_1} + \frac{V_B}{R_2}$$

$$\Rightarrow \frac{V_1}{R_1} + \frac{V_2}{R_2} = V_B\left[\frac{1}{R_1} + \frac{1}{R_2}\right]$$

$$= V_B\left[\frac{R_1 + R_2}{R_1 R_2}\right]$$

$$\Rightarrow V_B = \left[\frac{V_1}{R_1} + \frac{V_2}{R_2}\right] \frac{R_1 R_2}{R_1 + R_2}$$

$$= \left[\frac{V_1 R_2 + V_2 R_1}{R_1 R_2}\right] \cdot \frac{R_1 R_2}{R_1 + R_2}$$

$$\Rightarrow V_B = \frac{V_1 R_2 + V_2 R_1}{R_1 + R_2} \quad \text{—— (1)}$$

At node 'A'

$$I = \frac{V_0 - V_A}{R_f} = \frac{V_0 - V_B}{R_f} \quad \text{—— (2)} \qquad [\because V_A = V_B]$$

and

$$I = \frac{V_A - 0}{R} = \frac{V_A}{R} = \frac{V_B}{R} \quad \text{—— (3)} \qquad [\because V_A = V_B]$$

evaluate eq (2), (3)

$$\Rightarrow \frac{V_0 - V_B}{R_f} = \frac{V_B}{R}$$

$$\Rightarrow \frac{V_0}{R_f} - \frac{V_B}{R_f} = \frac{V_B}{R}$$

$$\Rightarrow \frac{V_0}{R_f} = \frac{V_B}{R} + \frac{V_B}{R_f}$$

$$= V_B\left[\frac{1}{R}+\frac{1}{R_f}\right]$$

$$\frac{V_0}{R_f} = V_B\left[\frac{R_f+R}{RR_f}\right]$$

$$\Rightarrow V_0 = R_f \cdot V_B\left[\frac{R_f+R}{RR_f}\right]$$

$$\Rightarrow V_0 = V_B\left[\frac{R_f+R}{R}\right] \quad \text{— (4)}$$

sub. eq (1) in (4)

$$\Rightarrow V_0 = \left[\frac{V_1R_2+V_2R_1}{R_1+R_2}\right]\left[\frac{R_f+R}{R}\right]$$

$$= \frac{V_1R_2}{R_1+R_2}\cdot\left[\frac{R_f+R}{R}\right] + \frac{V_2R_1}{R_1+R_2}\cdot\left[\frac{R_f+R}{R}\right]$$

$$V_0 = \frac{R_2(R_f+R)V_1}{R(R_1+R_2)} + \frac{R_1(R+R_f)V_2}{R(R_1+R_2)} \quad \text{— (5)}$$

If $R_1 = R_2 = R_f = R$,

then $\boxed{V_0 = V_1+V_2}$

There is no phase difference between Input and output.

Note

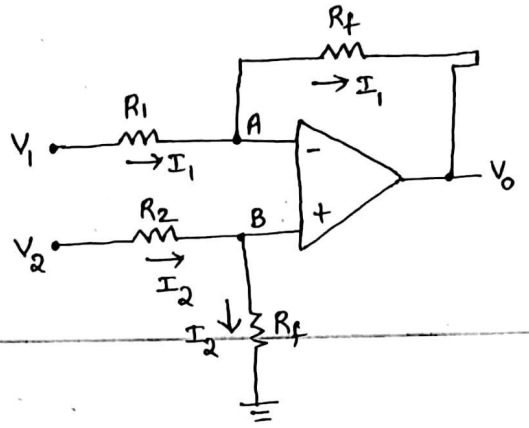
Average of Inverting Summer circuit $V_0 = -\left[\frac{V_1+V_2}{2}\right]$

The output voltage is average of 2 Input voltages so circuit called as averager.

Subtractor (or) Difference Amplifier :-

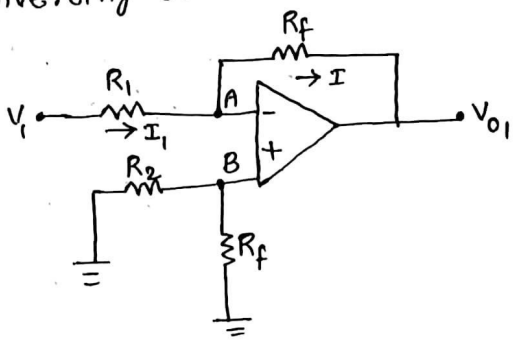
The subtraction of 2 Input voltages is possible with help of op-amp circuit is called subtractor (or) difference Amplifier.

method-1



To find relation between Inputs and output use super position principle.

case ①:- Input applied to Inverting terminal and V_2 considered to zero

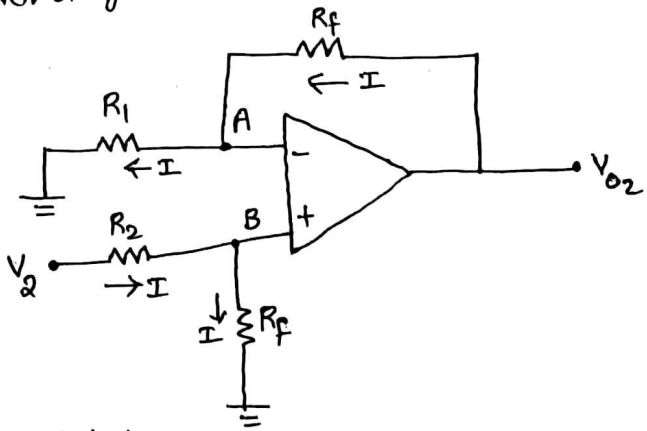


we know that,

Inverting OP-amp

$$V_{o_1} = -\frac{R_f}{R_1} \cdot V_1 \quad \text{—①}$$

case ②:- Input applied to Non-Inverting terminal and V_1 considered as zero.



It is Non-Inverting OP-Amp

$$V_{o_2} = \left(1 + \frac{R_f}{R_1}\right) V_B \quad \text{—②}$$

Apply voltage divider rule at Node 'B',

$$V_B = \left(\frac{R_f}{R_2 + R_f}\right) V_2 \quad \text{—③}$$

sub. eqv ③ in eqv ②

$$V_{o2} = \left(1 + \frac{R_f}{R_1}\right) \frac{R_f V_2}{R_2 + R_f} \quad \text{—④}$$

According to super position principle,

$$V_o = V_{o1} + V_{o2}$$

$$= -\frac{R_f}{R_1} V_1 + \left[1 + \frac{R_f}{R_1}\right] \cdot \frac{R_f V_2}{R_2 + R_f}$$

$$= -\frac{R_f}{R_1} V_1 + \left[\frac{R_1 + R_f}{R_1}\right] \frac{R_f V_2}{R_2 + R_f}$$

If $R_1 = R_2 = R_f = R$, then

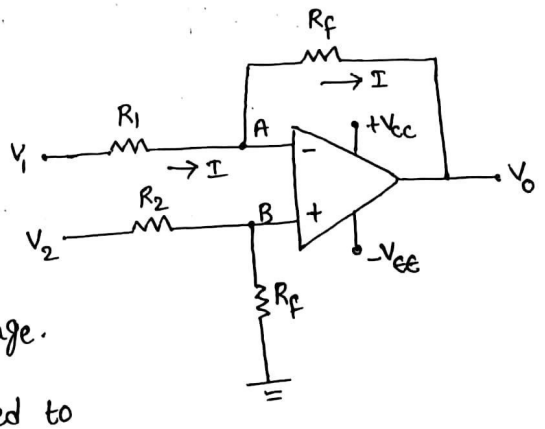
$$V_o = -V_1 + V_2$$

$$\Rightarrow \boxed{V_o = V_2 - V_1}$$

The output voltage is proportional to the difference between 2 voltages.

(or)

method-2 :-



V_1, V_2 are Input voltages and V_o is the output voltage.

→ The output voltage connected to Inverting terminal through R_f. So It is -ve feed back and current $I_A = 0$, $I_B = 0$

i) $I_A = 0, I_B = 0$

ii) $V_B = V_A$ [∵ concept of virtual ground]

suppose, Input applied to Inverting terminal so, $V_B = 0$.

If $V_B = 0$ it act as open circuit.

voltage divider rule at 'B',

$$V_B = \frac{R_f}{R_f + R_2} V_2 \quad \text{—①}$$

At Node 'A'

Input side, $I = \frac{V_1 - V_A}{R_1}$ —②

output side, $I = \frac{V_A - V_0}{R_f}$ —③

equate eq ②, ③

$$\frac{V_1 - V_A}{R_1} = \frac{V_A - V_0}{R_f}$$

$$\Rightarrow (V_1 - V_A) R_f = (V_A - V_0) R_1$$

$$\Rightarrow V_1 R_f - V_A R_f = V_A R_1 - V_0 R_1$$

$$\Rightarrow V_0 R_1 = V_A R_1 - V_1 R_f + V_A R_f$$

$$= V_A (R_1 + R_f) - V_1 R_f$$

$$\Rightarrow V_0 = \frac{V_A}{R_1} (R_1 + R_f) - \frac{V_1}{R_1} R_f \quad \text{—④}$$

If $V_B = V_A$,

Sub. eq ① in ④

$$\Rightarrow V_0 = \left(\frac{R_f}{R_f + R_2}\right) V_2 \frac{(R_1 + R_f)}{R_1} - \frac{V_1}{R_1} R_f$$

consider $R_1 = R_2$

$$\Rightarrow V_o = \left(\frac{R_f}{R_f + R_1}\right) V_2 \cdot \left[\frac{R_1 + R_f}{R_1}\right] - V_1 \frac{R_f}{R_1}$$

$$= \frac{R_f V_2}{R_1} - \frac{V_1 R_f}{R_1}$$

$$V_o = \frac{R_f}{R_1}(V_2 - V_1)$$

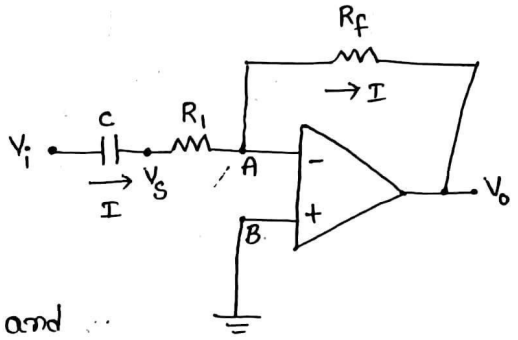
If $R_1 = R_f$

$$\Rightarrow \boxed{V_o = V_2 - V_1}$$

A.c Amplifier :-

The op-amp can Amplify A.c signals is called A.c Amplifier.

1. Inverting A.c Amplifier :-



The Input applied to Inverting terminal and Input consists of A.c signal and D.c signals.

→ The capacitor is used to block d.c signals and Allows only A.c Signals.

we know that, $V_o = -\frac{R_f}{R_1} \cdot V_s$ —①

From fig②,

$$I = \frac{V_i}{R_1 + C} = \frac{V_i}{R_1 + \frac{1}{j\omega C}} \quad —②$$

and $V_s = IR_1$ —③

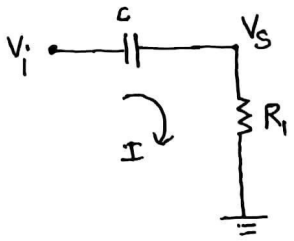


Fig :-②

Sub. eqn ② in eqn ③,

$$V_s = \left[\frac{V_i}{R_1 + \frac{1}{j\omega C}} \right] R_1$$

$$= \frac{V_i R_1}{R_1\left[1 + \frac{1}{j\omega C R_1}\right]} = \frac{V_i}{1 + \frac{1}{j\omega C R_1}} = \frac{V_i}{1 + \frac{j}{j\omega C R_1 \cdot j}}$$

$$= \frac{V_i}{1 + \frac{j}{j^2 2\pi f C R_1}}$$

$$= \frac{V_i}{1 - \frac{j}{2\pi f R_1 C}} \quad [\because j^2 = -1]$$

Let $f_L = \frac{1}{2\pi R_1 C}$

$$\Rightarrow V_s = \frac{V_i}{1 - j\left(\frac{f_L}{f}\right)} \quad \text{—④}$$

Sub. eqn ④ in ①

$$\Rightarrow V_o = -\frac{R_f}{R_1}\left[\frac{V_i}{1 - j(f_L/f)}\right]$$

$$\Rightarrow \frac{V_o}{V_i} = -\frac{R_f}{R_1}\left[\frac{1}{1 - j(f_L/f)}\right]$$

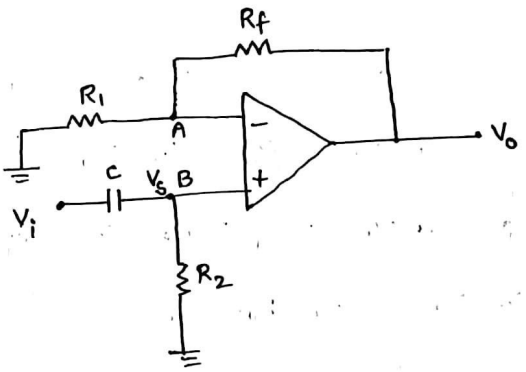
magnitude is $\left|\frac{V_o}{V_i}\right| = -\frac{R_f}{R_1} \cdot \frac{1}{\sqrt{1 + (f_L/f)^2}}$

$$= -\frac{R_f}{R_1} \cdot \frac{1}{\sqrt{1+0}} \quad \left[\because f << f_L \text{ (or) } \frac{f_L}{f} >> 1\right]$$

$$\boxed{A_{CL} = -\frac{R_f}{R_1}} \quad \text{—⑤}$$

The coupling capacitor C_c controls the low frequency limit.

2. Non-Inverting A.C Amplifier :-



we know that,

$$\frac{V_o}{V_s} = 1 + \frac{R_f}{R_1}$$

$$\Rightarrow V_o = \left(1 + \frac{R_f}{R_1}\right) V_s \quad \text{—⑥}$$

Sub. eqn ④ in ⑥

$$\Rightarrow V_o = \left(1 + \frac{R_f}{R_1}\right) \left[\frac{V_i}{1 - j(f_L/f)}\right]$$

$$\Rightarrow \frac{V_o}{V_i} = \left(1 + \frac{R_f}{R_1}\right) \left[\frac{1}{1 - j(f_L/f)}\right]$$

magnitude, $\left|\frac{V_o}{V_i}\right| = \left(1 + \frac{R_f}{R_1}\right) \frac{1}{\sqrt{1 + \left(\frac{f_L}{f}\right)^2}}$

If $f << f_L$ (or) $\frac{f_L}{f} >> 1$

$$\Rightarrow \boxed{A = 1 + \frac{R_f}{R_1}} \quad \text{—⑦}$$

The lower cut-off frequency again controlled by coupling capacita C_c.

3. A.C Voltage follower :-

The capacitors used to Allows A.C signals only.

→ The output voltage follows the Input.

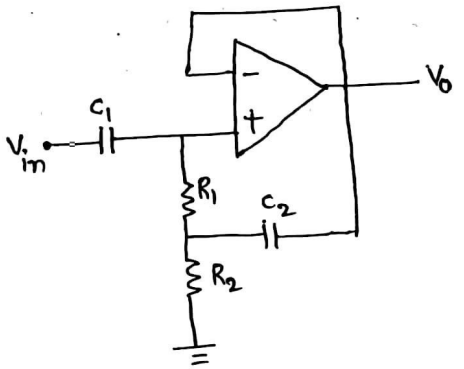
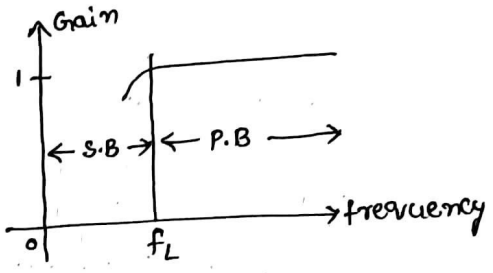


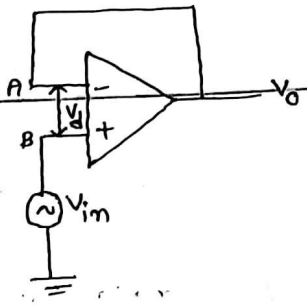
Fig :- A.C voltage follower.

The frequency response characteristics are

→ The frequencies below f_L can not be Allowed so it indicates "stop band" and allows only higher frequencies indicates "pass band".



Voltage follower (Buffer):-



The output follows Input so it gives voltage follower.

From fig. $V_B = V_{in}$

$\Rightarrow V_A = V_{in}$ $[\because V_A = V_B]$

$\Rightarrow V_A = V_B = V_{in}$

$\Rightarrow \boxed{V_o = V_{in}}$

The characteristics are

i) Gain = 1

ii) Input resistance '∞'

iii) output resistance '0'.

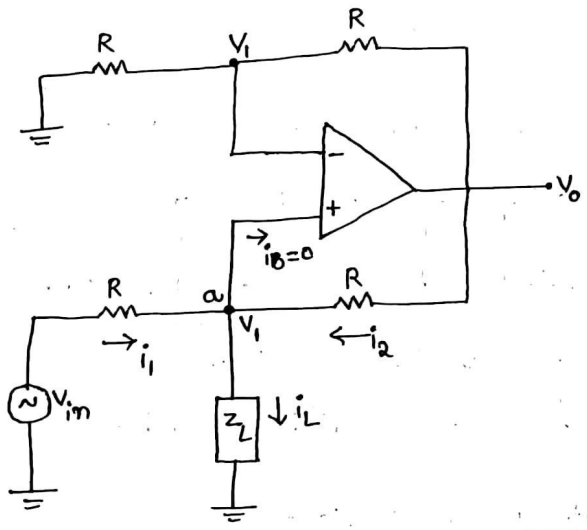


Fig:- V-I converter with grounded load.

From the figure,

$$i_1 = \frac{V_{in} - V_1}{R} \quad \text{and} \quad i_2 = \frac{V_o - V_1}{R}$$

Apply KCL at node 'a'

$$i_1 + i_2 = i_L \quad \text{—①}$$

$$\Rightarrow \frac{V_{in} - V_1}{R} + \frac{V_o - V_1}{R} = i_L$$

$$\Rightarrow V_{in} - V_1 + V_o - V_1 = i_L R$$

$$\Rightarrow V_{in} + V_o - 2V_1 = i_L R \quad \text{—②}$$

$$\Rightarrow V_1 = \frac{V_{in} + V_o - i_L R}{2} \quad \text{—③}$$

In this circuit, OP-Amp is connected to Non-Inverting mode we know that gain of the circuit is

$$A = 1 + \frac{R_f}{R}$$

In this circuit, $R_f = R$

$$\Rightarrow A = 1 + \frac{R}{R} \Rightarrow A = 2 \Rightarrow \frac{V_o}{V_{in}} = 2. \quad \left[\because A = \frac{V_o}{V_{in}}\right]$$

$\Rightarrow V_0 = 2V_1$ — ③

sub. eq ③ in ②

$\Rightarrow V_{in} + 2V_1 - 2V_1 = i_L R$

$\Rightarrow V_{in} = i_L R \quad \Rightarrow \boxed{i_L = \frac{V_{in}}{R}}$

Applications:-

→ used in LEDs.

→ used as Low voltage dc and AC voltmeter

→ zener diode tester.

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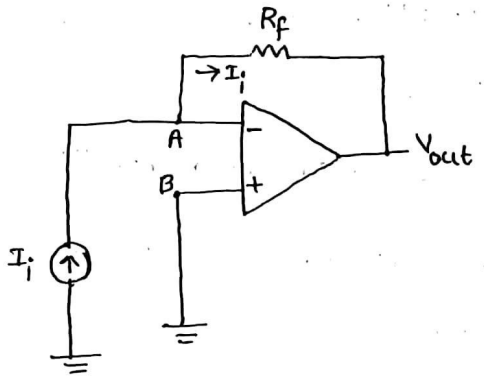
current to voltage converter (Transresistance Amplifier):-

The circuit which converts the Input current into output voltage is called current to voltage converter.

→ The output voltage of I/V converter is directly proportional to Input current.



From fig. $V_B = 0$

concept of virtual ground

$V_A = 0$

At node A,

$$I_i = \frac{V_A - V_{out}}{R_f} = \frac{0 - V_{out}}{R_f} = \frac{-V_{out}}{R_f}$$

$$\Rightarrow \boxed{V_{out} = -I_i R_f}$$

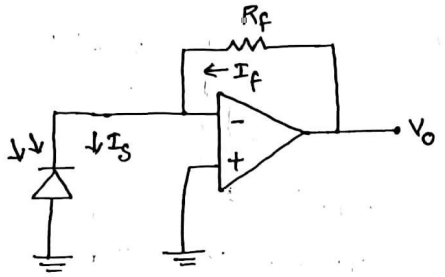
$$\Rightarrow V_{out} \propto I_i$$

Thus, output voltage is proportional to Input current and circuit works as current to voltage converter. It also refered as current controlled voltage source (ccvs).

Applications:-

1. photo diode detector
2. photo FET detector

Photo diode detector:-



The photo diode produces electrical current in response to Incident light. This current flows through R_f. The voltage across R_f, the output voltage is proportional to diode current.

Instrumentation Amplifier :-

The Amplifier which is used for low level Amplification with high cmRR, high Input Impedance to avoid loading, low power consumption and some other features is called Instrumentation Amplifier.

→ It also called data Amplifier.

→ The Important features (or) characteristics of Instrumentation Amplifier are

i) high gain Accuracy
ii) high cmRR
iii) High Input Impedance
iv) Low output Impedance
v) Low power consumption
vi) high gain stability with low temp. coefficient
vii) High slew rate

Fig. shows difference Amplifier.

we know that,

From difference Amplifier

$$V_o = \frac{R_f}{R_1}(V_2 - V_1) \quad \text{—①}$$

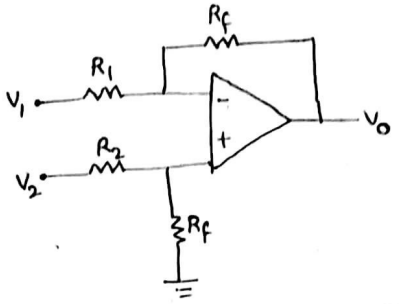


Fig:- Differential Amplifier using single OP-Amp

Three OP-Amp Instrumentation Amplifier :-

This circuit provides high Input resistance for Accurate measurement of signals from transducers.

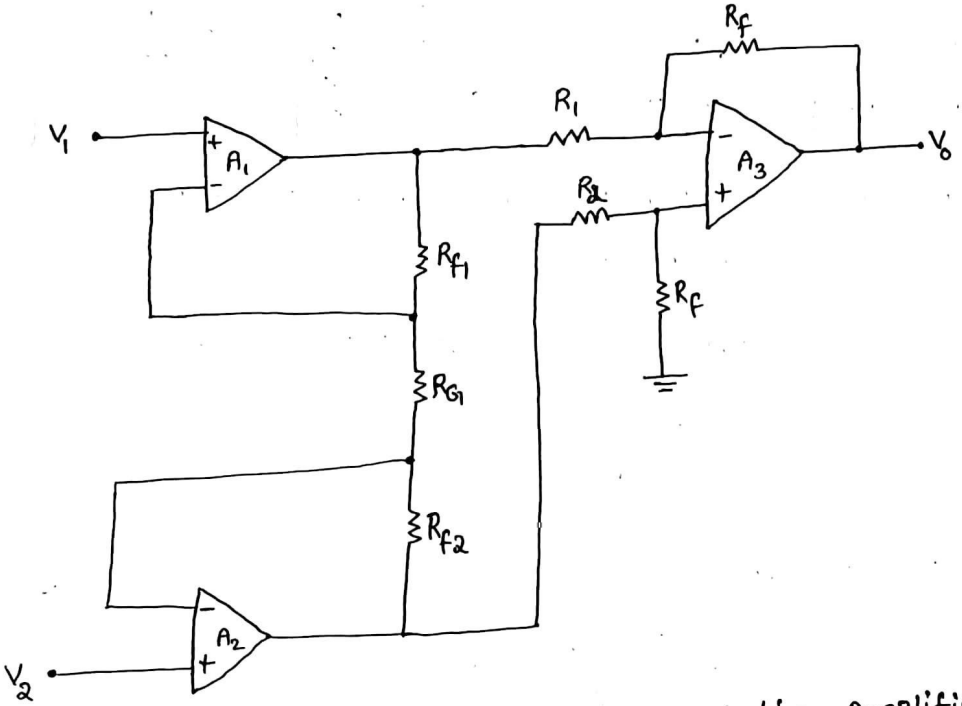


Fig :- Three OP-Amp Instrumentation Amplifier

It contains 2 stages, Input and output stage

→ Input stage contains 2-opamps A_1, A_2 are used for high Input Impedance. [2-OP-amps are identical, I/P's connected to Non-Inverting termin

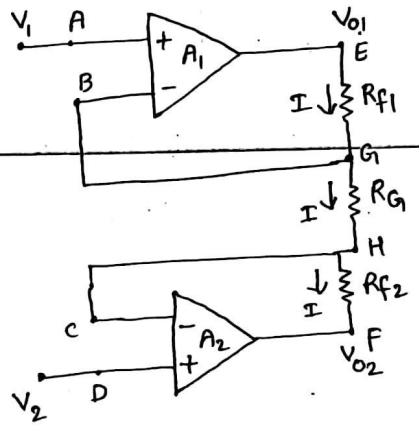
→ output stage contains op-amp A_3 it is difference Amplifier.

Analysis :-

From the circuit, output stage is similar to basic difference Amplifier (or) subtractor.

w.k.t $V_0 = \frac{R_f}{R_1}(V_2 - V_1)$ — ②

Now consider first stage (or) Input stage.



→ Node 'A' potential of OP-Amp A_1 is V_1. so, Node 'B' is also V_1. hence potential of G is V_1.

→ Node 'D' potential of OP-amp A_2 is V_2. so, Node 'C' also V_2 and hence potential of H is V_2.

→ Input current of OP-amp A_1, A_2 both are zero. hence current I remains same through R_{f1}, R_G, R_{f2}.

Apply ohm's Law between nodes E, F we get,

$$I = \frac{V_{01} - V_{02}}{R_{f1} + R_G + R_{f2}} \quad \text{— ③}$$

Let $R_{f1} = R_{f2} = R_f$

$$\Rightarrow I = \frac{V_{01} - V_{02}}{2R_f + R_G} \quad \text{— ④}$$

At Nodes G and H,

$$I = \frac{V_G - V_H}{R_G} = \frac{V_1 - V_2}{R_G} \quad \text{— ⑤} \qquad [\because V_G = V_1, \; V_H = V_2]$$

equating eq ④, ⑤

$$\frac{V_{01} - V_{02}}{2R_f + R_G} = \frac{V_1 - V_2}{R_G}$$

$$\Rightarrow \frac{V_{o2}-V_{o1}}{2R_f+R_{G_1}} = \frac{V_2-V_1}{R_{G_1}} \quad \text{—⑥}$$

$$\Rightarrow V_{o2}-V_{o1} = \frac{(2R_f+R_{G_1})(V_2-V_1)}{R_{G_1}} \quad \text{—⑦}$$

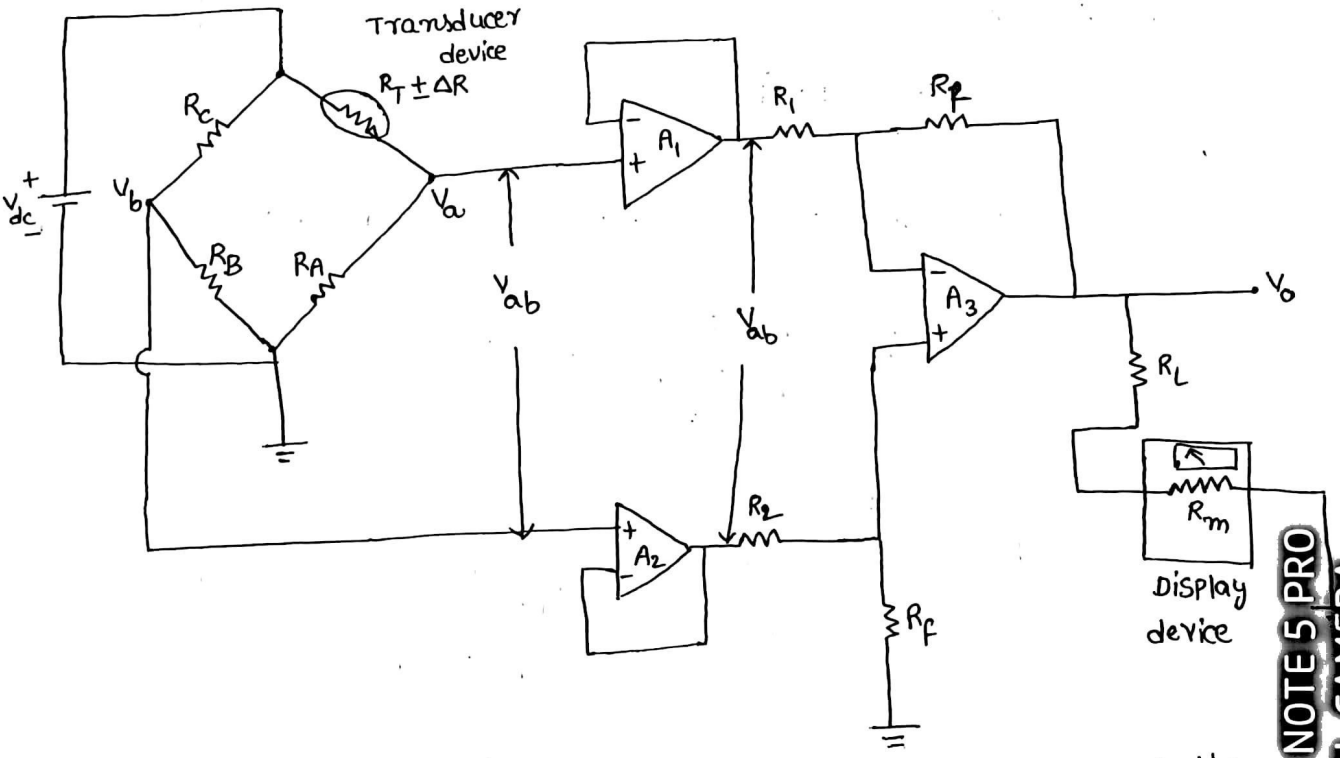
Sub. eq⑦ in eq②,

$$\Rightarrow V_o = \frac{R_f}{R_1}\left[\frac{(2R_f+R_{G_1})(V_2-V_1)}{R_{G_1}}\right]$$

$$\boxed{V_o = \frac{R_f}{R_1}\left(1+\frac{2R_f}{R_{G_1}}\right)(V_2-V_1)} \quad \text{—⑧}$$

This is the overall gain of the circuit.

Instrumentation Amplifier using transducer bridge :-



R_T be the resistance of the transducer device which is one of the arms of the resistive bridge, while ΔR is the change in resistance R_T. So, effective resistance of transducer is $R_T \pm \Delta R$.

The bridge balanced condition, is

$$\frac{R_C}{R_B} = \frac{R_T}{R_A} \quad \text{—①}$$

This condition is generally established by the designer and depends on transducer device characteristics, type of the physical energy to be measured and desired application.

When there is a change in physical quantity to be measured, the voltage V_a no longer remains same as V_b. This is due to fact that the resistance of transducer device changes from R_T to $R_T + \Delta R$. and hence balancing of the bridge gets disturbed. This produces differential Input for the Instrumentation Amplifier.

The resistances R_B, R_C are constant and voltage V_b will remain same,

$$V_b = \frac{R_B \cdot V_{dc}}{R_B + R_C} \quad \text{—②}$$

Due to change in resistance of the transducer device, V_a becomes

$$V_a = \frac{R_A (V_{dc})}{R_A + R_T + \Delta R} \quad \text{—③}$$

$$\therefore V_{ab} = V_b - V_a$$

$$= \frac{R_B \cdot V_{dc}}{R_B + R_C} - \frac{R_A \cdot V_{dc}}{R_A + R_T + \Delta R} \quad \text{—④}$$

If $R_A = R_B = R_C = R_T = R$, then

$$V_{ab} = \frac{R V_{dc}}{2R} - \frac{R V_{dc}}{2R + \Delta R}$$

$$V_{ab} = \frac{RV_{dc}(2R+\Delta R) - RV_{dc}(2R)}{2R(2R+\Delta R)}$$

$$= \frac{2R^2 V_{dc} + R\Delta R V_{dc} - 2R^2 V_{dc}}{2R(2R+\Delta R)}$$

$$\Rightarrow V_{ab} = \frac{\Delta R V_{dc}}{2(2R+\Delta R)} \quad \text{——⑤}$$

The +ve V_{ab} i.e $V_b - V_a$ indicates $V_b > V_a$

Now the gain of 1st stage of Instrumentation amplifier is unity as its voltage follower circuit and gain of 2nd stage is $-R_f/R_1$

$$\therefore V_o = V_{ab} \times \left(-\frac{R_f}{R_1}\right)$$

$$= \frac{-R_f}{R_1}\left[\frac{\Delta R V_{dc}}{2(2R+\Delta R)}\right]$$

AS $\Delta R << 2R$, neglecting it

$$\Rightarrow V_o = -\frac{R_f}{R_1}\frac{\Delta R}{4R} \cdot V_{dc} \quad \text{——⑥}$$

Thus, the output voltage is proportional to change in resistance ΔR. Thus the meter connected to output can be calibrated in terms of units of physical quantity to be measured.

In general, gain of Instrumentation amplifier whether it is any instrumentation Amplifier circuit,

$$V_o = \frac{A\,\Delta R}{4R} V_{dc} \quad \text{——⑦} \qquad \left[\because A = -\frac{R_f}{R_1}\right]$$

Applications:-

1) Temperature Indicator
2) Temperature controller
3) Light Intensity meter
4) Analog weight scale.

Comparators:-

A circuit which compares a signal voltage applied at one Input and reference voltage at other Input and produces output voltage.

The output voltage is high value (or) low value depending upon Input.

$V_N \rightarrow$ Voltage of Inverting terminal

$V_p \rightarrow$ Voltage of Non Inverting terminal

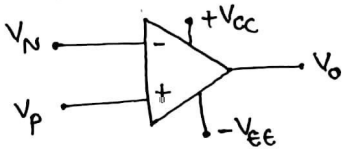


Fig:- op-amp as comparator

Two voltages compared with each other and V_o is either $+V_{sat}$ (or) $-V_{sat}$.

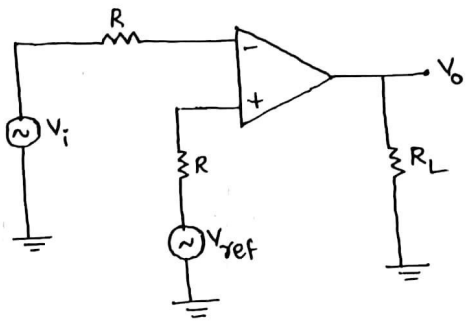
Depending upon terminals, they are classified into 2 types

i) Non Inverting comparator.

ii) Inverting comparator

1. Inverting comparator :-

The Input voltage is applied to Inverting terminal and reference voltage is applied to Non-Inverting terminal.



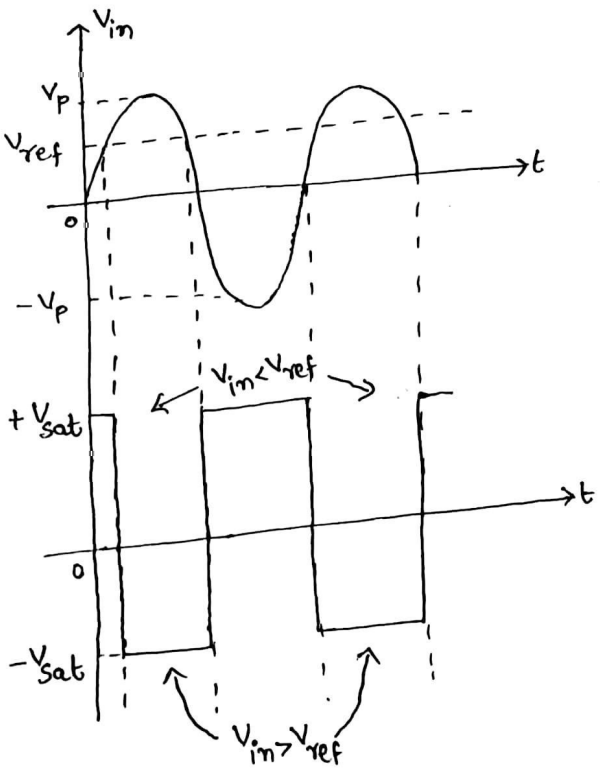
case 1 :- $V_{in} < V_{ref}$

In this case, the output voltage ~~$V_o = +V_{sat}$ $(+V_{cc})$~~

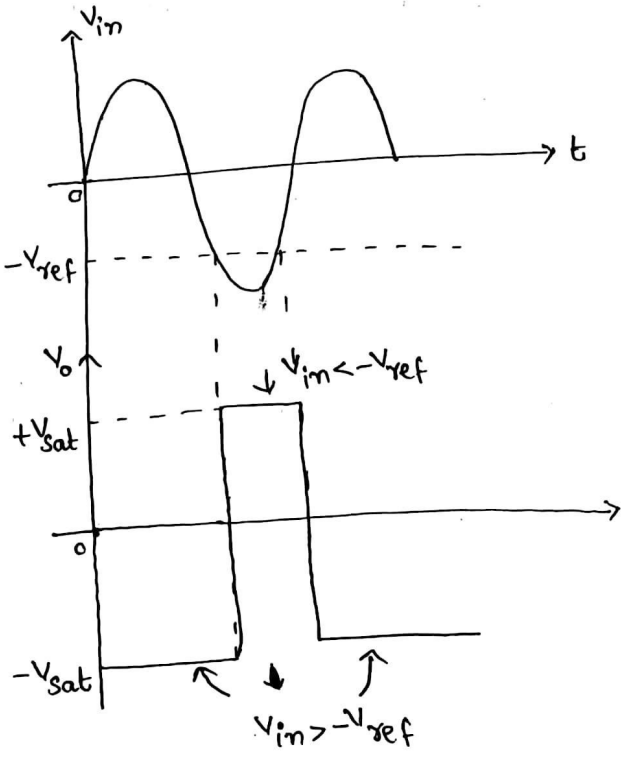
case 2 :- $V_{in} > V_{ref}$

In this case, the output voltage $V_o = -V_{sat}$ $(-V_{EE})$

Input and output waveforms :-

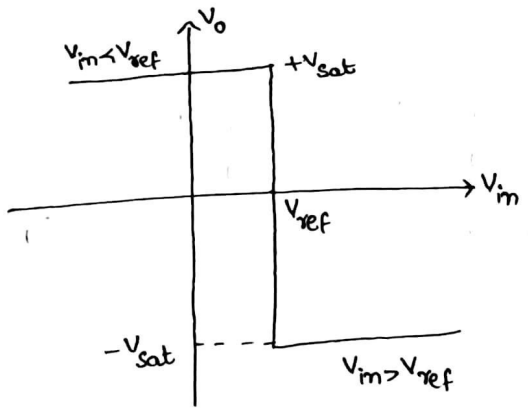


a) Taking +ve V_{ref}



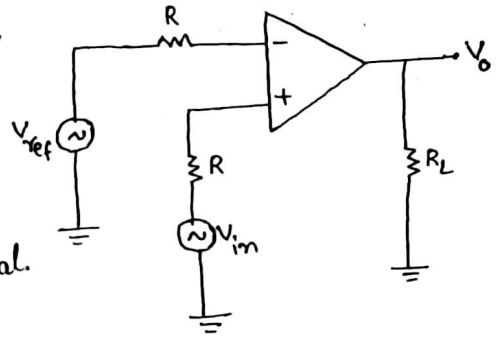
b) Taking $-V_{ref}$

Transfer characteristics :-



2. Non-Inverting comparator :-

In Non-Inverting comparator, Input V_{in} applied to Non-Inverting terminal and V_{ref} applied to Inverting terminal.



case ① $V_{in} > V_{ref}$

In this case, output voltage $V_o = V_{sat}$ $(+V_{cc})$

case ② $V_{in} < V_{ref}$

In this case, output voltage $V_o = -V_{sat}$ $(-V_{ee})$

Input and output waveforms :-

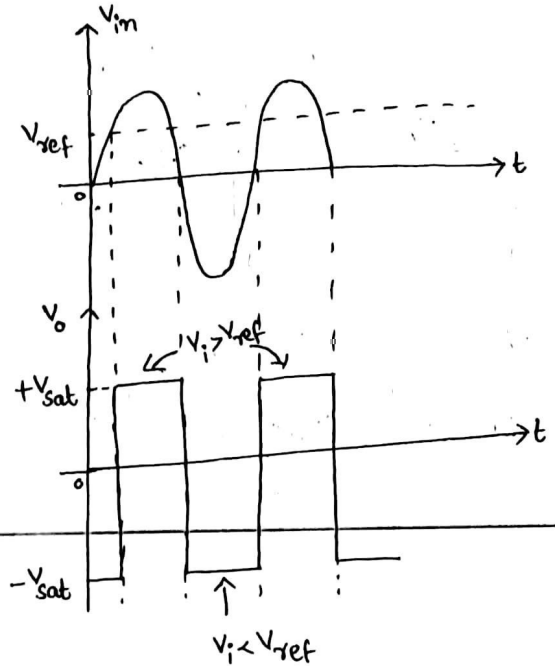


Fig :- Taking $+V_{ref}$

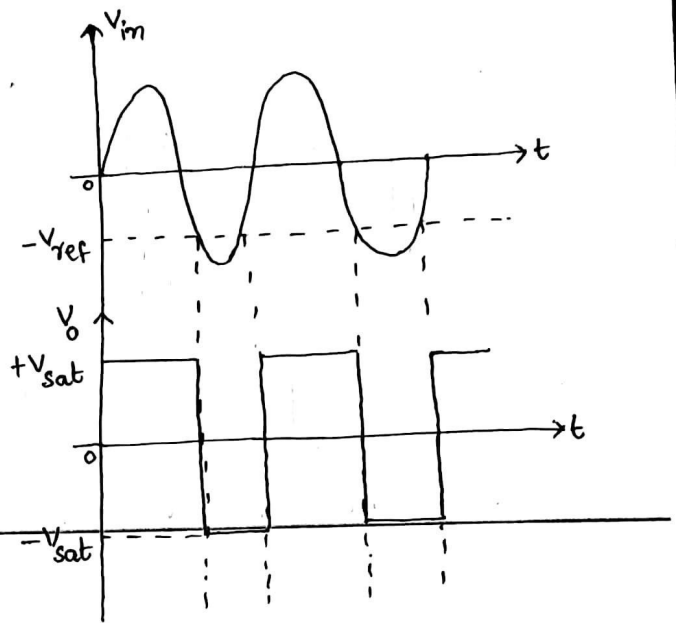
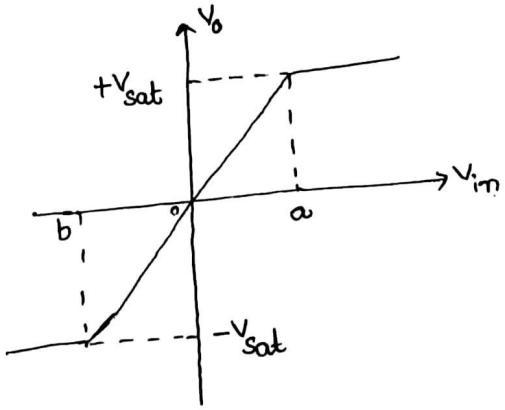


Fig :- Taking $-V_{ref}$

Transfer characteristics :-

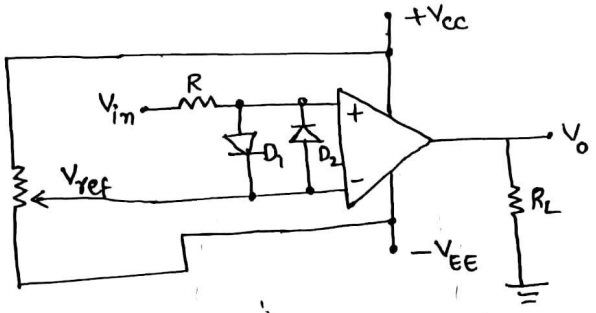


Practical comparator :-

The circuit consists of protective diodes and Potentiom to adjust the reference voltage.

The diodes D_1, D_2 are connected to protect the op-amp from damage due to Excessive input voltage V_{in}.

→ From these diodes, the difference Input voltage V_{id} always less than 0.7V (or) −0.7V



→ In case of Excess Input voltage, difference Input voltage V_{id} of the op-amp is clamped to either 0.7V (or) −0.7V due to forward biasing of diodes hence, these diodes are called clamp diodes.

Characteristics of comparator :-

→ Accuracy
→ Logic threshold
→ Strobe function
→ Response time
→ positive output level
→ Negative output level
→ Strobe current
→ strobe release time
→ Saturation voltage

Applications of comparator :-

1. zero crossing detector :-

During +ve half cycle, the input voltage is +ve ie above reference voltage the output is V_{sat}.

→ During -ve half cycle, Input voltage V_{in} is -ve i.e below reference voltage the output voltage is $-V_{sat}$.

→ The output voltage switches between $+V_{sat}$ and $-V_{sat}$ whenever the Input signal crosses the zero level.

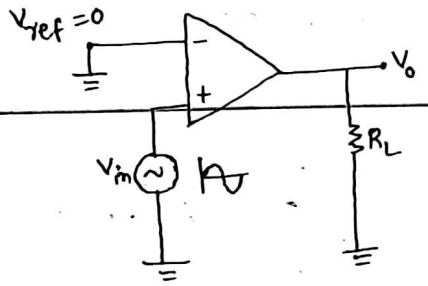
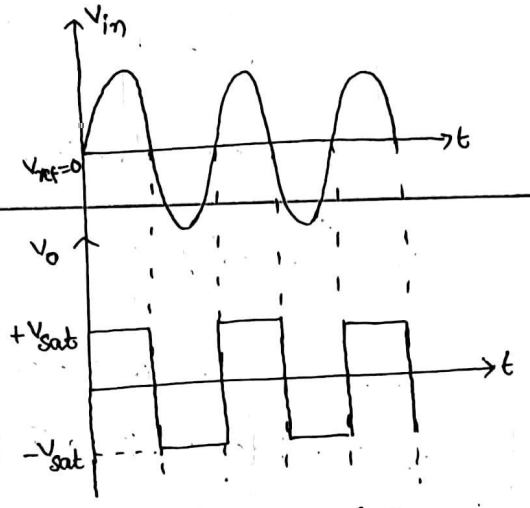


Fig:- zero-crossing detector



b) output waveform

Application :-

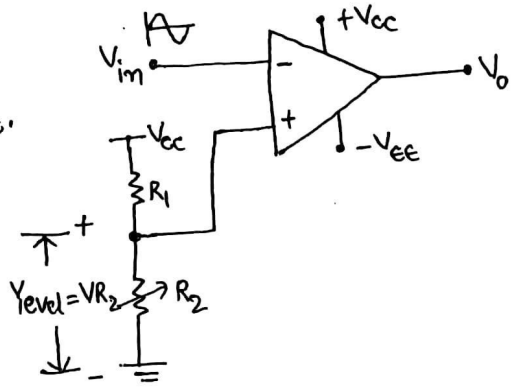
→ sine wave to square wave converter.

2) Level detector :-

The Non-Inverting terminal is biased to V_{level} voltage which is drop across R_2 can be set to a level to be detected.

→ AS V_{in} Increases above V_{level}, output changes from $+V_{sat}$ to $-V_{sat}$.

→ AS V_{in} falls below V_{level}, output changes from $-V_{sat}$ to $+V_{sat}$.



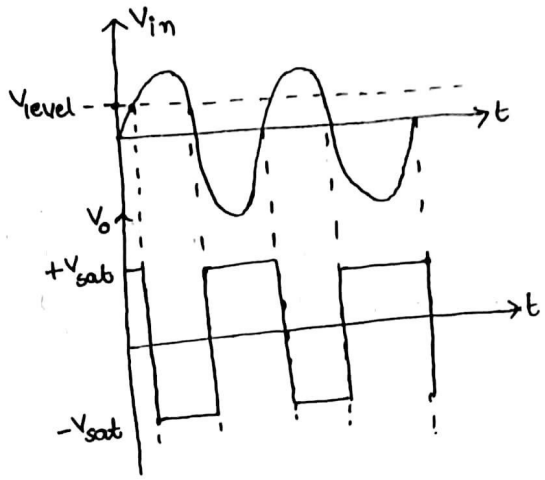
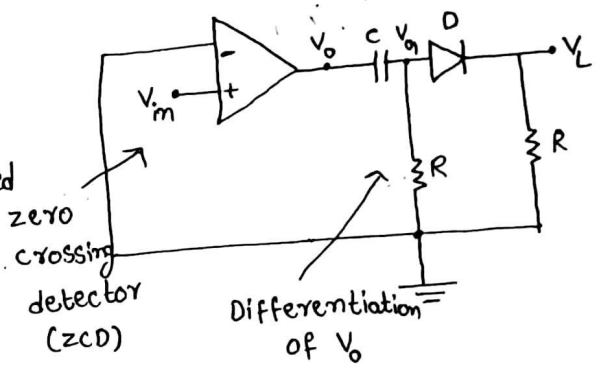
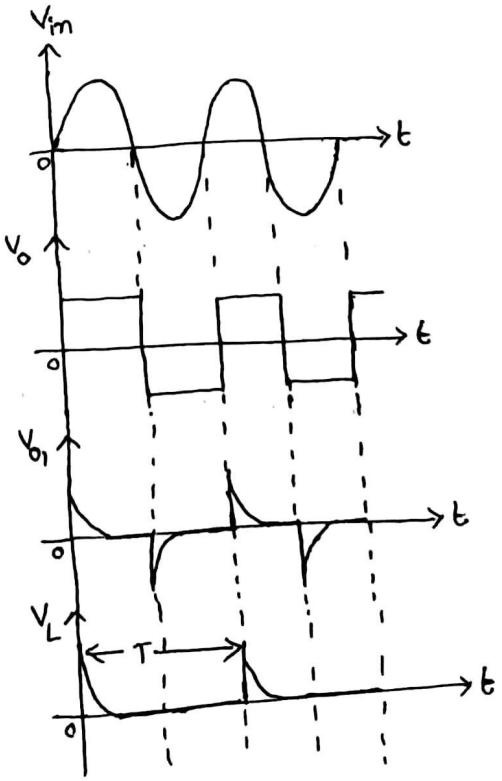


Fig:- waveforms of voltage level detector

3. Time marker generator :-

In this circuit, output of zero crossing detector is differentiated using Rc circuit. This produces train of +ve & -ve pulses denoted as V_{01} & -ve pulses can be eliminated using diode. Then the output is a train of +ve pulses.



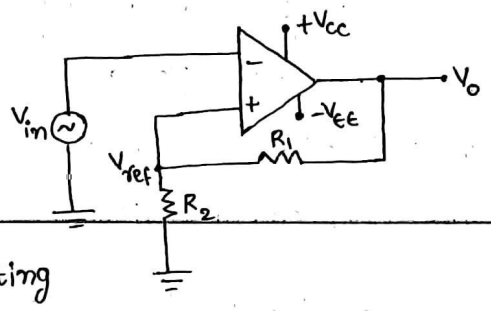


Regenerative comparator (schmitt trigger) :-

It is used to avoid unwanted noise, which is basically uses a +ve feed back.

1. Inverting schmitt trigger circuit :-

→ As the Input applied to Inverting terminal, produces opposite Polarity output.



→ This is feed back to Non-Inverting Input which is same Polarity of output.

case1 :- $V_{in} > V_{ref}$

The out Put goes to $-V_{sat}$.

case2 :- $V_{in} < V_{ref}$

The output goes to $+V_{sat}$.

→ The output voltage is always at $+V_{sat}$ and $-V_{sat}$.

Apply voltage divider at V_{ref}, then

$$+V_{ref} = \frac{R_2}{R_1+R_2} \cdot V_o = \frac{V_{sat}\, R_2}{R_1+R_2} \quad [\because V_o = +V_{sat}]$$

and

$$-V_{ref} = \frac{V_o R_2}{R_1+R_2} = \frac{-V_{sat}\, R_2}{R_1+R_2} \quad [\because V_o = -V_{sat}]$$

→ $+V_{ref}$ is +ve saturation when $V_o = +V_{sat}$ is called upper threshold voltage (V_{UT}).

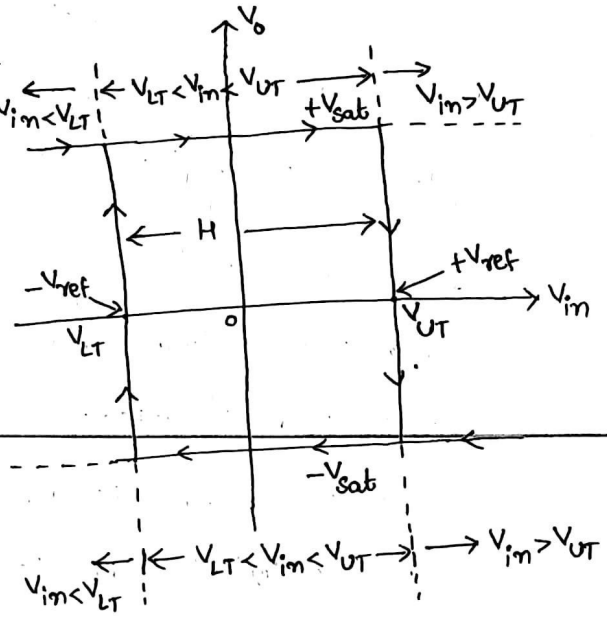
→ $-V_{ref}$ is -ve saturation when $V_o = -V_{sat}$ is called Lower threshold voltage (V_{LT}).

then, $V_{UT} = \frac{+V_{sat} R_2}{R_1 + R_2}$

$V_{LT} = \frac{-V_{sat} R_2}{R_1 + R_2}$

Transfer characteristics :-

→ The graph is drawn between Input voltage & output voltage is called ~~transfer characteristics~~.



→ output changes it state, there is a Input voltage crosses any of the threshold voltage levels. This is called "Hysteresis". It also called dead band (or) dead zone.

→ Difference between V_{UT} and V_{LT} is called width of hysteries denoted by H.

$$H = V_{UT} - V_{LT}$$

$$= \frac{V_{sat} R_2}{R_1 + R_2} - \left[\frac{-V_{sat} R_2}{R_1 + R_2}\right]$$

$$\boxed{H = \frac{2 V_{sat} R_2}{R_1 + R_2}}$$

→ AS $V_{in} > V_{UT}$ → output voltage $V_o = -V_{sat}$

→ AS $V_{in} < V_{UT}$ → output voltage $V_o = +V_{sat}$

→ $V_{LT} < V_i < V_{UT}$ → V_o = Previous state achieved.

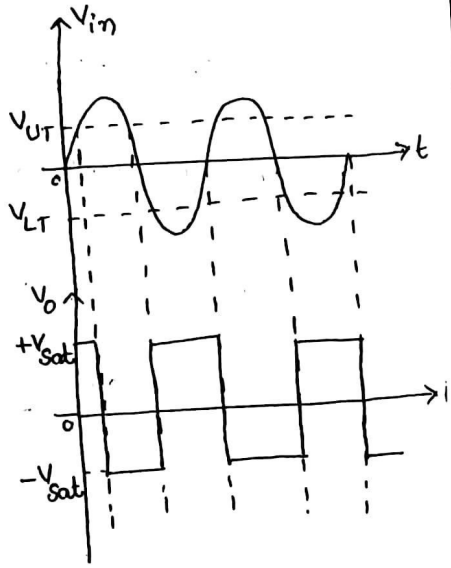
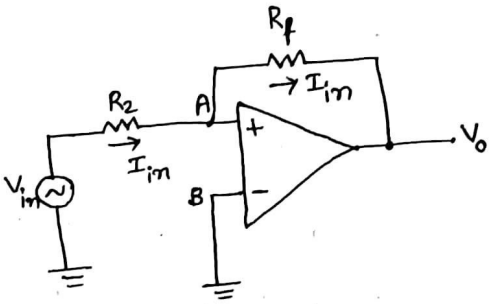


Fig :- Input & output waveforms

2. Non Inverting schmitt trigger :-

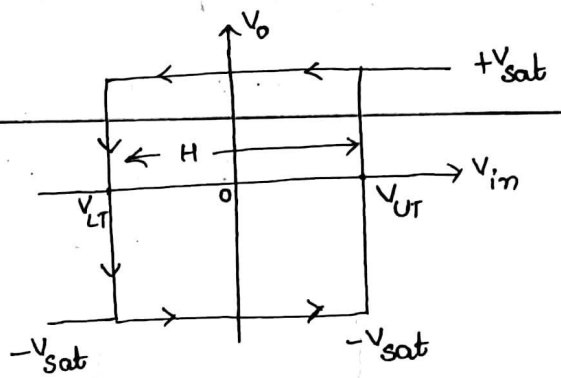


Input applied to Non-Inverting terminal.

→ AS $V_{in} > V_{UT}$ → output voltage $V_o = +V_{sat}$

→ AS $V_{in} < V_{UT}$ → output voltage $V_o = -V_{sat}$

Transfer characteristics :-



From fig, at Point 'A',

$V_A = I_{in} R_2$

$= V_{UT}$

From fig, $I_{in} = \frac{V_A + V_o}{R_1} = \frac{0 + V_o}{R_1} = \frac{V_o}{R_1}$ $[\because V_A = 0]$

$= +\frac{V_{sat}}{R_1}$

$\therefore V_{UT} = I_{in} R_2$

$= V_{sat} \cdot \frac{R_2}{R_1}$

and $V_{LT} = \frac{R_2}{R_1}(-V_{sat})$

$\therefore H = V_{UT} - V_{LT}$

$= V_{sat} \frac{R_2}{R_1} - \left[(-V_{sat}) \frac{R_2}{R_1}\right]$

$$\boxed{H = 2 V_{sat} \frac{R_2}{R_1}}$$

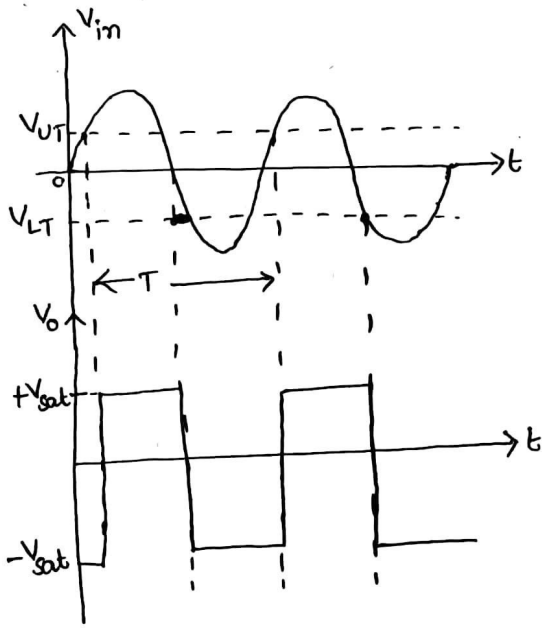
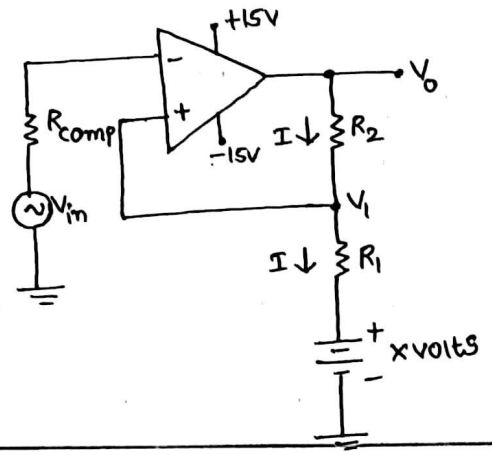


Fig :- Input and output waveform

Schmitt trigger with different UTP and LTP Levels :-

In this circuit, an additional voltage source of 'x' volts connected in series between R_1 & ground.

→ The voltage V_1 depends on 'x' and decides UTP and LTP levels.



Apply KVL to output circuit,

$$V_o - IR_2 - IR_1 - x = 0$$

$$\Rightarrow V_o = I(R_1 + R_2) + x$$

$$\Rightarrow I = \frac{V_o - x}{R_1 + R_2} \quad \text{—①}$$

and $V_1 = IR_1 + x$ —②

sub. eq① in ②

$$V_1 = \left[\frac{V_o - x}{R_1 + R_2}\right] R_1 + x \quad \text{—③}$$

For $V_1 = V_{UT}$, $V_o = +V_{sat}$

$$V_{UT} = \left[\frac{V_{sat} - x}{R_1 + R_2}\right] R_1 + x \quad \text{—④}$$

For $V_1 = V_{LT}$, $V_o = -V_{sat}$

$$V_{LT} = \left[\frac{-V_{sat} - x}{R_1 + R_2}\right] R_1 + x \quad \text{—⑤}$$

Subtracting eq⑤ from eq④

$$V_{UT} - V_{LT} = \frac{V_{sat} - x}{R_1 + R_2} \cdot R_1 + x - \left[\frac{-V_{sat} - x}{R_1 + R_2} \cdot R_1 + x\right]$$

$$= \frac{2V_{sat} R_1}{R_1 + R_2} \quad \text{—⑥}$$

From eq⑥, $R_{comp} = R_1 \| R_2$

Multivibrators using op-amp :-

These are used in timing Applications. The multivibrators are classified as

1. monostable multivibrators
2. Astable multivibrators

1. monostable multivibrators :- (or) one-shot multivibrator :-

It contains one stable state and one quasi stable state. when an External trigger is applied, the output changes it state from stable state to quasistable state. after some time it return back to its original state. usually, the charging and discharging of a capacitor Provides this Internal trigger signal.

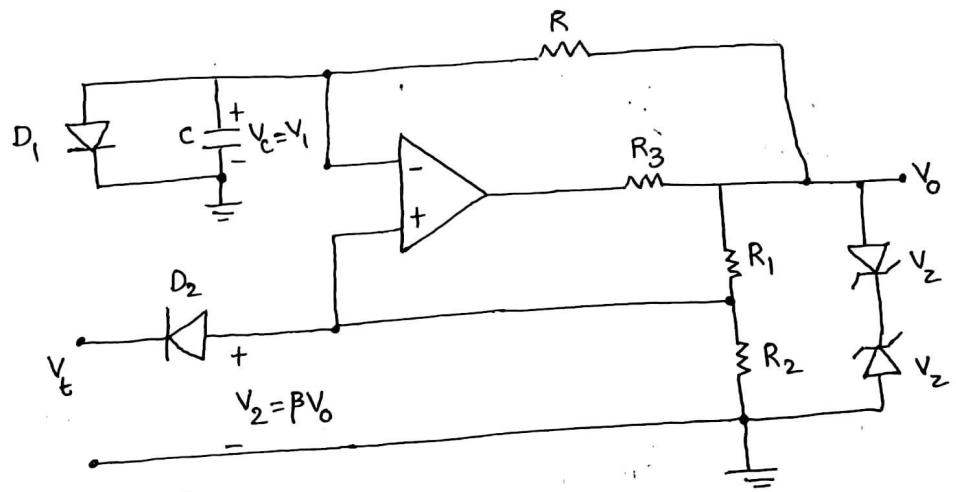


Fig :- OP-Amp monostable multivibrator

Operation :-

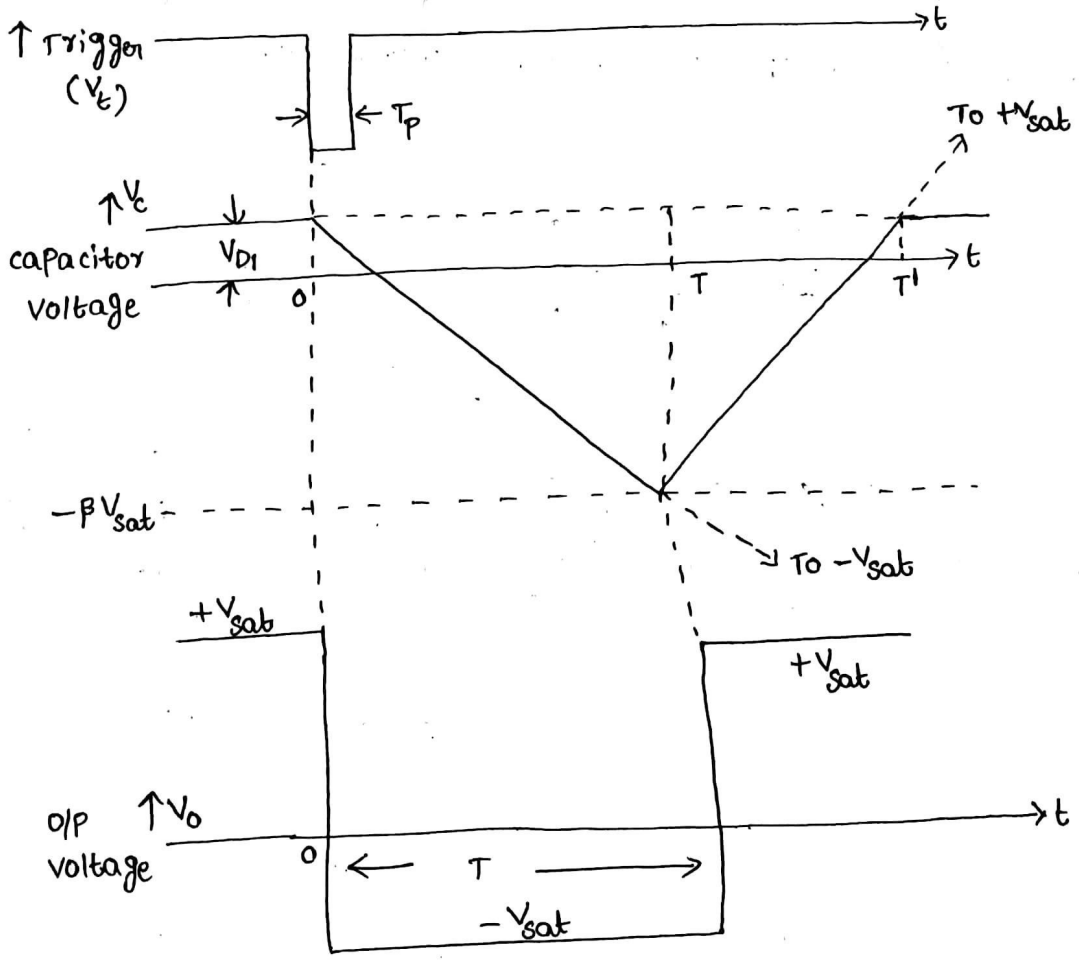
Let us assume that output V_o is at $+V_{sat}$ i.e in stable state. The diode D_1 conducts and voltage across capacitor is V_c

gets clamped to 0.7V. Voltage at non Inverting terminal is βV_{sat} in the stable state.

→ If V_t, -ve voltage applied to Non-Inverting terminal then the output of OP-Amp changes its state from $+V_{sat}$ to $-V_{sat}$. diode is reverse biased and capacitor starts charging exponentially to $-V_{sat}$. The voltage at Non Inverting terminal is now $-\beta V_{sat}$.

→ when the capacitor voltage V_c becomes more negative than $-\beta V_{sat}$, output of OP-amp changes its state back to $+V_{sat}$.

waveforms :-



Expression for pulse width (T):-

W.K.T $V_0 = V_f - (V_f - V_{in})\, e^{-t/RC}$ — ①

where, $V_0 = V_c$, $V_{in} = V_{D1}$, $V_f = -V_{sat}$

$\Rightarrow V_c = -V_{sat} - (-V_{sat} - V_{D1})\, e^{-t/RC}$

At $t = T$, $V_c = -\beta V_{sat}$

$\Rightarrow -\beta V_{sat} = -V_{sat} + (V_{sat} + V_{D1})\, e^{-T/RC}$

$\Rightarrow (V_{sat} + V_{D1})\, e^{-T/RC} = -V_{sat}\cdot\beta + V_{sat}$

$= V_{sat}(1-\beta)$

$\Rightarrow e^{-T/RC} = \dfrac{V_{sat}(1-\beta)}{V_{sat} + V_{D1}}$

$\Rightarrow e^{T/RC} = \dfrac{V_{sat} + V_{D1}}{V_{sat}(1-\beta)}$

Apply 'ln' on both sides,

$$T/RC = \ln\left(\frac{V_{sat} + V_{D1}}{V_{sat}(1-\beta)}\right)$$

$$\Rightarrow T = RC \ln\left[\frac{V_{sat} + V_{D1}}{V_{sat}(1-\beta)}\right] = RC \ln\left[\frac{V_{sat}\left(1 + \frac{V_{D1}}{V_{sat}}\right)}{V_{sat}(1-\beta)}\right]$$

$$T = RC \ln\left(\frac{1 + \frac{V_{D1}}{V_{sat}}}{1-\beta}\right) \quad \text{— ②}$$

At $V_{sat} >> V_{D1}$, From fig. $\beta = \dfrac{R_2}{R_1 + R_2}$,

If $R_1 = R_2$ then $\beta = \dfrac{R_1}{2R_1} = \dfrac{1}{2} = 0.5$

sub. 'β' value in eqv ②,

$$\Rightarrow T = RC \ln\left[\frac{1}{1-0.5}\right] \qquad [\because V_{sat} >> V_{D1}]$$

$$= RC \ln\left[\frac{1}{0.5}\right]$$

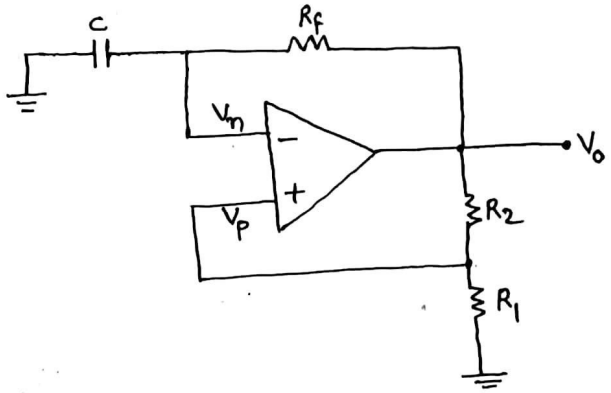
$$= RC \ln(2)$$

$$\boxed{T = 0.69\,RC}$$

2. Astable multivibrator :- (or) free running multivibrator :-

→ It contains 2 quasi-stable states and No stable states i.e circuit oscillate between 2 quasi stable states.

→ No External trigger is applied to changes the states.



The circuit looks like a comparator (schmitt trigger) except that Input voltage is replaced by a capacitor.

i) when V_o is at $+V_{sat}$

Feed back voltage is called upper threshold voltage V_{UT}

$$\text{i.e } V_{UT} = \frac{R_1 (+V_{sat})}{R_1 + R_2} \quad \text{—①}$$

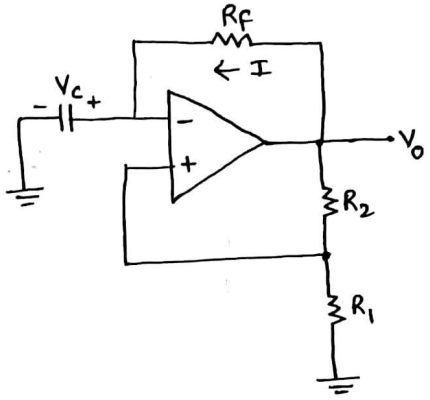
ii) when V_o is at $-V_{sat}$

Feed back voltage is called Lower threshold voltage V_{LT}

$$\text{i.e } V_{LT} = \frac{R_1 (-V_{sat})}{R_1 + R_2} \quad \text{—②}$$

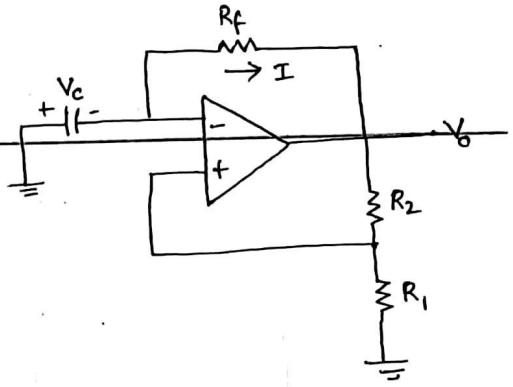
i) when $V_o = +V_{sat}$:-

In this case, capacitor starts charging towards $+V_{sat}$ through the feedback path provided by resistor R_f to Inverting Input.



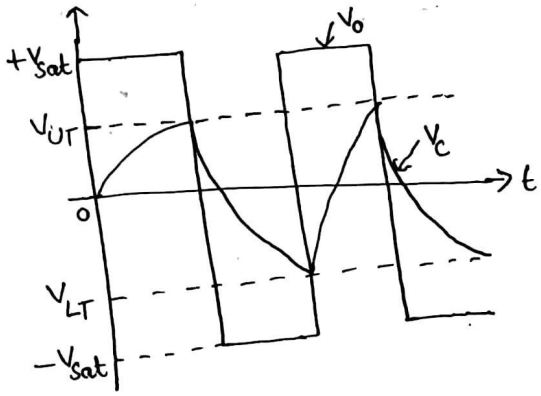
ii) when $V_o = -V_{sat}$:-

In this case, capacitor starts discharging towards $-V_{sat}$ through the feedback path provided by resistor R_f.



Output waveforms :-

The Initial voltage V_{LT} & capacitor discharge from V_{LT} to 0V and recharge to V_{UT} the process is repeating.



Frequency of oscillation :-

we know that,

$$V_o = V_f - (V_f - V_{in})\, e^{-t/RC} \quad \text{—①}$$

From fig, $V_{in} = V_{LT}$, $V_f = V_{UT} + V_{sat}$, $V_o = V_{UT}$

$$V_{UT} = V_{sat} - (V_{sat} - V_{LT})\, e^{-T_1/RC} \qquad [\because t = T_1]$$

$$\Rightarrow (V_{sat} - V_{LT})\, e^{-T_1/RC} = V_{sat} - V_{UT}$$

$$\Rightarrow e^{-T_1/RC} = \frac{V_{sat} - V_{UT}}{V_{sat} - V_{LT}}$$

$$\Rightarrow e^{T_1/RC} = \frac{V_{sat} - V_{LT}}{V_{sat} - V_{UT}}$$

Apply 'ln' on both sides,

$$\frac{T_1}{RC} = \ln\left(\frac{V_{sat} - V_{LT}}{V_{sat} - V_{UT}}\right)$$

$$\Rightarrow T_1 = RC \ln\left(\frac{V_{sat} - V_{LT}}{V_{sat} - V_{UT}}\right) \quad \text{---②}$$

consider $T = 2T_1$, because capacitor charge from V_{UT} to V_{LT} is same as time required for charging capacitor from V_{LT} to V_{UT}

$$\Rightarrow T = 2RC \ln\left[\frac{V_{sat} - V_{LT}}{V_{sat} - V_{UT}}\right] \quad \text{---③}$$

and $f = \dfrac{1}{2RC \ln\left[\frac{V_{sat} - V_{LT}}{V_{sat} - V_{UT}}\right]}$

Sub. V_{UT} and V_{LT} in eq ③,

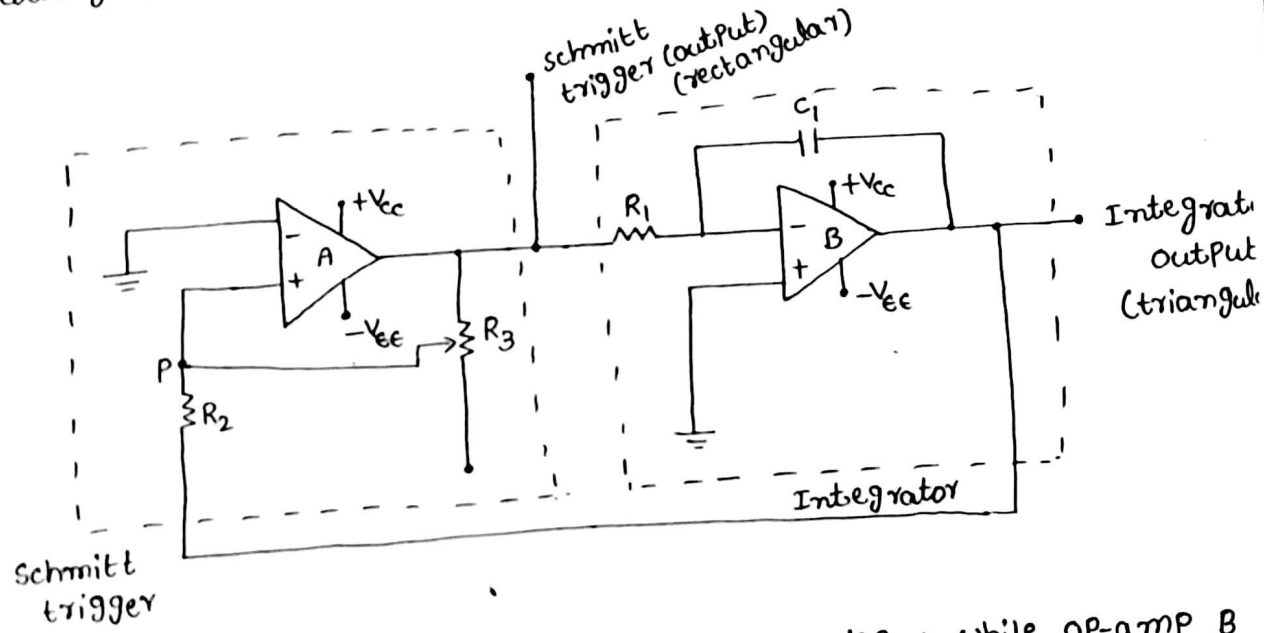
$$T = 2RC \ln\left[\frac{V_{sat} - (R_1 x - V_{sat})/R_1 + R_2}{V_{sat} - (R_1 x + V_{sat})/R_1 + R_2}\right]$$

magnitudes of $+V_{sat}$ & $-V_{sat}$ are equal

$$\Rightarrow T = 2RC \ln\left[\frac{V_{sat}\left(1 + \frac{R_1}{R_1 + R_2}\right)}{V_{sat}\left(1 - \frac{R_1}{R_1 + R_2}\right)}\right] \Rightarrow \boxed{T = 2RC \ln\left(\frac{2R_1 + R_2}{R_2}\right)}$$

Triangular / rectangular wave generator :-

The output of Integrator is triangular if its Input is square wave input. while output of a schmitt trigger is square wave for any Input. Thus if output of schmitt trigger is applied to Input of Integrator and output of Integrator as Input to Schmitt trigger then circuit works as triangular / rectangular wave generator.



The OP-amp A circuit is schmitt trigger while op-amp B is an Integrator. The output of schmitt trigger is rectangular wave applied to Inverting Input of Integrator and produces triangular wave output.

Operation :-

Let the output of schmitt trigger is $+V_{sat}$. This forces cur... $+V_{sat}/R_1$ through C_1, charging C_1 with Polarity +ve to left & -V... in right

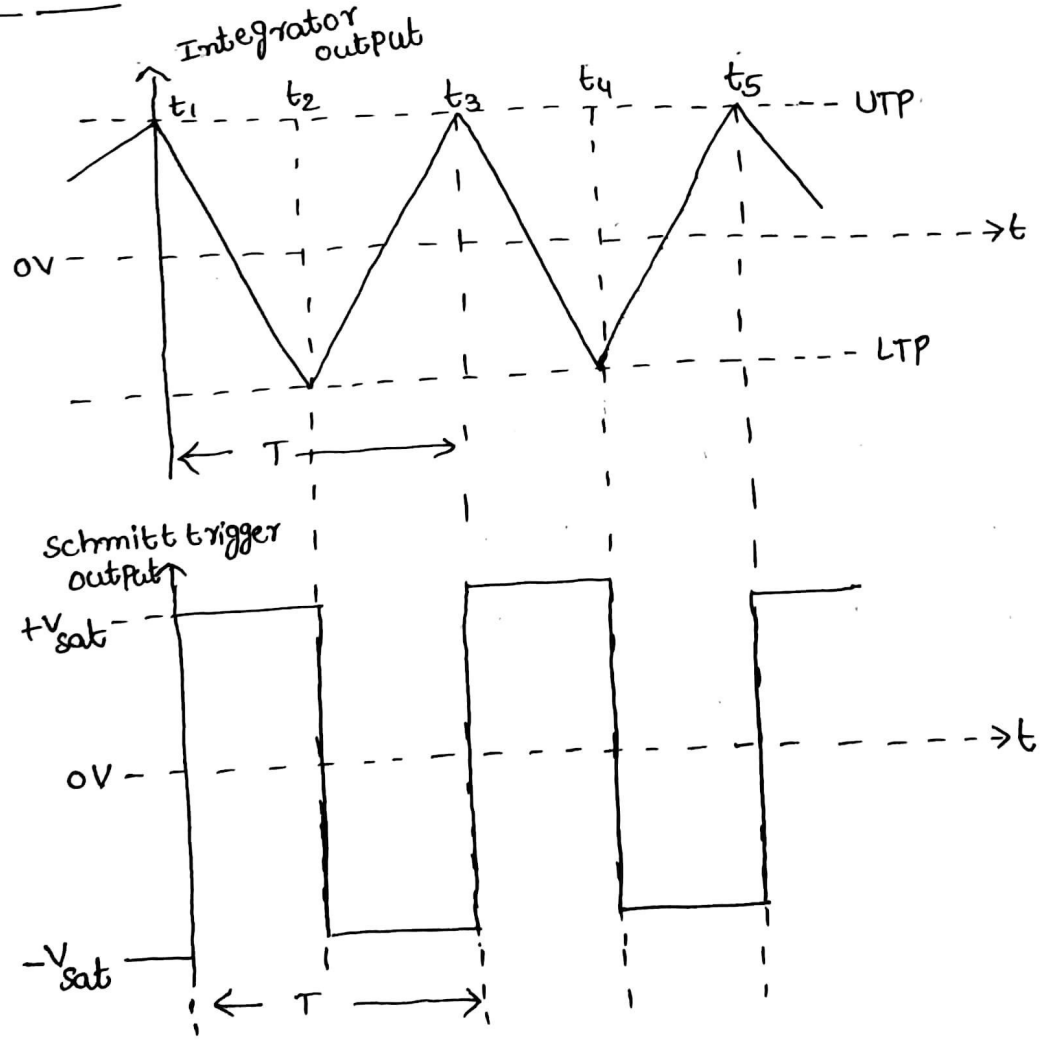
It produces -ve going ramp at its output, for the Interval t_1 to t_2

→ At t_2, when ramp voltage equal to LTP of schmitt trigger, output of schmitt trigger changes its state from $+V_{sat}$ to $-V_{sat}$.

→ Now direction of current through C_1 reverses. It discharges and recharges in opposite direction with polarity +ve to right and -ve to left. This produces +ve going ramp at its output, for the Interval t_2 to t_3.

→ At t_3, when ramp voltage equal to UTP of schmitt trigger, output of schmitt trigger changes its state from $-V_{sat}$ to $+V_{sat}$.

Wave forms :-



when the schmitt trigger output is at $+V_{sat}$, effective voltage at point 'p' is

$$-V_{ramp} + \frac{R_2}{R_2+R_3}\left[+V_{sat} - (-V_{ramp})\right] \quad -(1)$$

when the effective voltage at 'p' becomes zero, ie

$$-V_{ramp} + \frac{R_2}{R_2+R_3}\left[+V_{sat} - (-V_{ramp})\right] = 0$$

$$-V_{ramp} + \frac{R_2}{R_2+R_3}(V_{ramp}) + \frac{R_2}{R_2+R_3}(V_{sat}) = 0$$

$$V_{ramp}\left[-1 + \frac{R_2}{R_2+R_3}\right] = -\frac{R_2}{R_2+R_3}(V_{sat})$$

$$V_{ramp}\left[\frac{-R_2-R_3+R_2}{R_2+R_3}\right] = -\frac{R_2}{R_2+R_3}(V_{sat})$$

$$V_{ramp}\left[\frac{-R_3}{R_2+R_3}\right] = -\frac{R_2}{R_2+R_3}V_{sat}$$

$$\Rightarrow -V_{ramp} = -\frac{R_2}{R_3}V_{sat} \quad \text{---} (2)$$

$\frac{1}{2}$y output is at $-V_{sat}$, $+V_{ramp} = -\frac{R_2}{R_3}(-V_{sat})$ —(3)

Peak to Peak amplitude of triangular wave is given by

$$V_{out(P-P)} = +V_{ramp} - (-V_{ramp})$$

$$= -\frac{R_2}{R_3}V_{sat} - \left[-\frac{R_2}{R_3}V_{sat}\right] \quad \text{---} (4)$$

If $|+V_{sat}| = |-V_{sat}|$, then

$$V_{out(P-P)} = \frac{R_2}{R_2}V_{sat} + \frac{R_2}{R_2}V_{sat} = \frac{2R_2}{R_2}V_{sat} \quad \text{---} (5)$$

The time taken by the output to swing from $-V_{ramp}$ to $+V_{ramp}$ is equal to half the time period $T/2$.

$$V_{out(P-P)} = -\frac{1}{R_1C_1}\int_0^{T/2}(-V_{sat})\,dt$$

$$= \frac{V_{sat}}{R_1C_1}\int_0^{T/2} dt = \frac{V_{sat}}{R_1C_1}(t)_0^{T/2}$$

$$= \frac{V_{sat}}{R_1C_1}\left(\frac{T}{2}\right) \quad \text{—⑥}$$

$$\Rightarrow \boxed{T = \frac{V_{out(P-P)} \cdot 2R_1C_1}{V_{sat}}} \quad \text{—⑦}$$

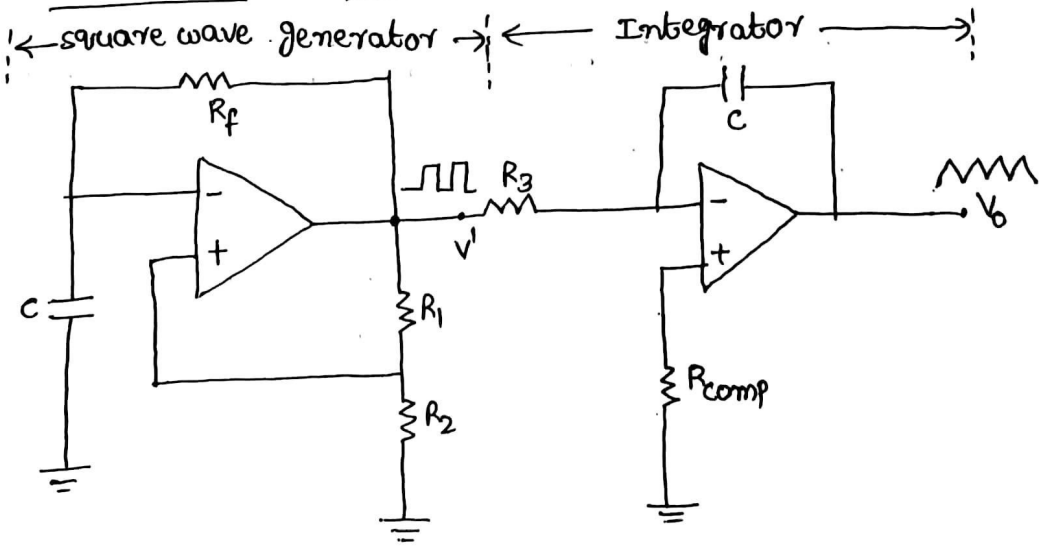
sub. eq ⑤ in ⑦,

$$T = \frac{\left\{\frac{2R_2}{R_3}V_{sat}\right\} \cdot 2R_1C_1}{V_{sat}}$$

$$T = \frac{4R_1R_2C_1}{R_3} \quad \text{—⑧}$$

∴ frequency of oscillation $\boxed{f_0 = \frac{R_3}{4R_1R_2C_1}}$ —⑨

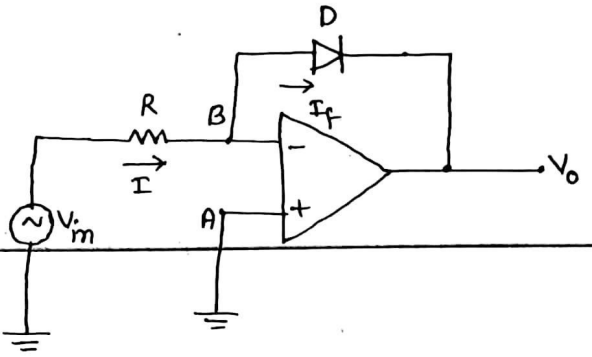
Another form of Triangular wave generator :-



Log Amplifiers :-

The circuit whose output is proportional to the logarithm of applied Input voltage is called "logarithmic Amplifier".

i) Log Amplifier using diode :-



From fig, $V_A = 0$

concept of virtual ground

$V_B = 0$

$\therefore I = \frac{V_{in} - V_B}{R} = \frac{V_{in}}{R}$ —①

w.k.t diode equation, $I = I_0 (e^{V/\eta V_T} - 1)$

Forward current is, $I_f = I_0 e^{V/\eta V_T}$ —② $\quad [\because 1 << e^{V/\eta V_T}]$

Taking 'ln' on both sides,

$$\ln[I_f] = \ln[I_0 e^{V/\eta V_T}]$$

$$= \ln[I_0] + \ln[e^{V/\eta V_T}]$$

$$= \ln[I_0] + V/\eta V_T$$

$$\Rightarrow \frac{V}{\eta V_T} = \ln[I_f] - \ln[I_0]$$

$$\Rightarrow V = \eta V_T [\ln[I_f] - \ln[I_0]]$$

$$\Rightarrow V = \eta V_T \ln\left[\frac{I_f}{I_0}\right] \quad —③$$

From fig, $I_f = V_B - V_o$

$= 0 - V_o = -V_o$ —④

(or) $\quad [\because V_B = V_i + V_o \quad 0 = V_i + V_o \Rightarrow V_i = -V_o]$

$\therefore$ eq③ can be $-V_o = \eta V_T \ln\left[\frac{I_f}{I_0}\right]$ —⑤

Sub. $I_f = I = \frac{V_{in}}{R}$ then eqv (5) changes to

$$V_o = -\eta V_T \ln\left[\frac{V_{in}}{RI_o}\right] \quad \text{—(6)}$$

consider $V_{ref} = R \cdot I_o$ then eqv (6) changes to

$$V_o = -\eta V_T \ln\left[\frac{V_{in}}{V_{ref}}\right] \quad \text{—(7)}$$

Thus, output voltage is proportional to logarithm of Input voltag

~~The circuit gives natural log (ln), one can find $\log_{10}$ by~~

Proper scaling as,

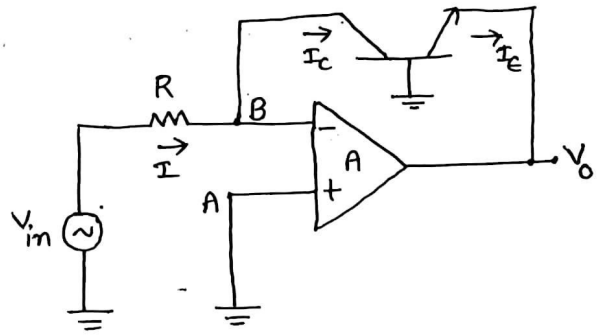
$$\log_{10} x = 0.4343 \ln(x)$$

ii) Log Amplifier using transistor:-

From fig, $V_A = 0$

concept of virtual ground

$V_B = 0$



and current,

$$I = \frac{V_{in} - V_B}{R} = \frac{V_{in}}{R} \quad \text{—(1)}$$

w.k.T, the equation for collector current in BJT,

$$I_c = -I_S\left(e^{V_{BE}/V_T} - 1\right)$$

$$I_c = -I_S\left(e^{V_{BE}/V_T}\right) \qquad \left[\because 1 << e^{V_{BE}/V_T}\right]$$

Taking 'ln' on both sides

$$\ln(I_c) = \ln\left[I_S\left(e^{V_{BE}/V_T}\right)\right]$$

$$\Rightarrow \ln\left[\frac{I_c}{I_s}\right] = \frac{V_{BE}}{V_T}$$

$$\Rightarrow V_{BE} = V_T \ln\left[\frac{I_c}{I_s}\right] \quad \text{—— (2)}$$

From fig, $V_B = V_0 + V_{BE}$

$$0 = V_0 + V_{BE}$$

$$\Rightarrow V_0 = -V_{BE} \quad \text{— (3)}$$

and current $I = I_c = \frac{V_{in}}{R}$ — (4)

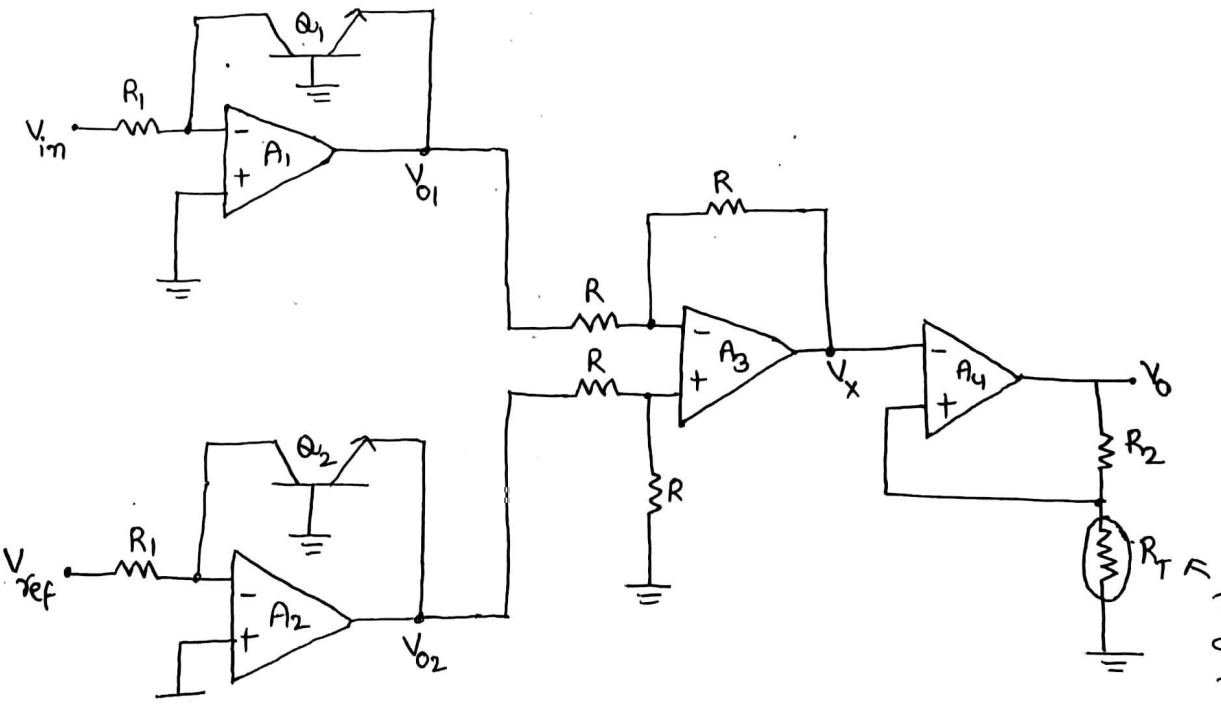
Sub. eq (3), (4) in eq (2)

$$\Rightarrow -V_0 = V_T \ln\left[\frac{V_{in}}{R I_s}\right] \quad \text{—(5)}$$

Let $I_s R = V_{ref}$, then eq (5) changes to

$$\boxed{V_0 = -V_T \ln\left[\frac{V_{in}}{V_{ref}}\right]}$$

iii) Temperature compensated Log Amplifier :-



→ In this technique, 2 log amplifiers are used. one used for reference voltage V_{ref} and other used for V_{in}.

→ Two transistors used in the two log Amplifier circuits are Integrated close together in the same silicon wafer. This Provides a close match of saturation currents and ensures good thermal tracking.

Assume, $I_{S_1} = I_{S_2} = I_S$ —①

voltages $V_{01} = -V_T \ln\left[\frac{V_{in}}{R_1 I_S}\right]$ —②

$V_{02} = -V_T \ln\left[\frac{V_{ref}}{R_1 I_S}\right]$ —③

OP-Amp A_3 act as difference Amplifier,

$$V_x = V_{02} - V_{01}$$

$$= -V_T \ln\left[\frac{V_{ref}}{R_1 I_S}\right] - \left[-V_T \ln\left[\frac{V_{in}}{R_1 I_S}\right]\right]$$

$$= -V_T \left[\ln\left(\frac{V_{ref}}{R_1}\right) + \ln\left(\frac{1}{I_S}\right) - \ln\left(\frac{V_{in}}{R_1}\right) - \ln\left(\frac{1}{I_S}\right)\right]$$

$$= -V_T \left[\ln\left[\frac{V_{ref}}{R_1}\right] + \ln\left[\frac{R_1}{V_{in}}\right]\right]$$

$$V_x = -V_T \ln\left[\frac{V_{ref}}{V_{in}}\right] \quad —④$$

(or)

$$V_x = V_T \ln\left[\frac{V_{in}}{V_{ref}}\right] \quad —⑤$$

V_{ref} is decided by external battery & it is not temp. dependent.

Last stage of OP-Amp A_4 it act as Non-Inverting Amplifier with gain of $\left(1+\frac{R_2}{R_T}\right)$

$\therefore$ output voltage $V_0 = V_x\left(1+\frac{R_2}{R_T}\right)$

$$= \frac{(R_2+R_T)}{R_T} \ln\left(\frac{V_{in}}{V_{ref}}\right) \quad \text{—— ⑥}$$

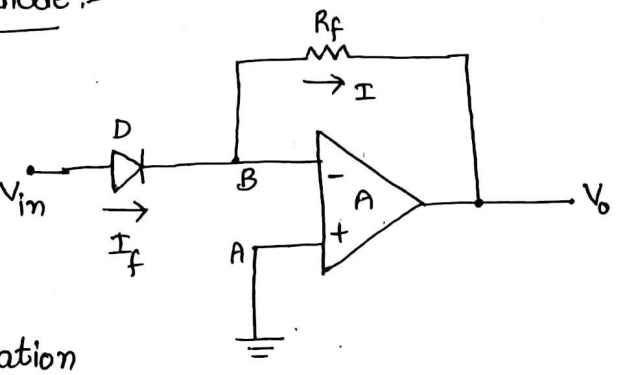
where R_T is $^{+ve}_{x}$ temperature coefficient (sensistor).

From eq ⑥, output voltage is proportional to logarithm of Input and temperature independent.

Antilog Amplifier :-

The log Amplifier can easily turned around to provide the Antilog (or) exponential function is called "Antilog Amplifier".

i) Anti log Amplifier using diode :-



From fig, $V_A = 0$

concept of virtual ground, V_{in}

$V_B = 0$

w.k.T, diode current equation

$$I_f = I_0 e^{V_{in}/\eta V_T} \quad \text{—— ①}$$

From fig, $I = I_f = \frac{V_B - V_0}{R_f} = \frac{-V_0}{R_f}$ —— ② $\quad [\because V_B = 0]$

equating eq ①, ②

$$I_0 e^{V_{in}/\eta V_T} = \frac{-V_0}{R_f}$$

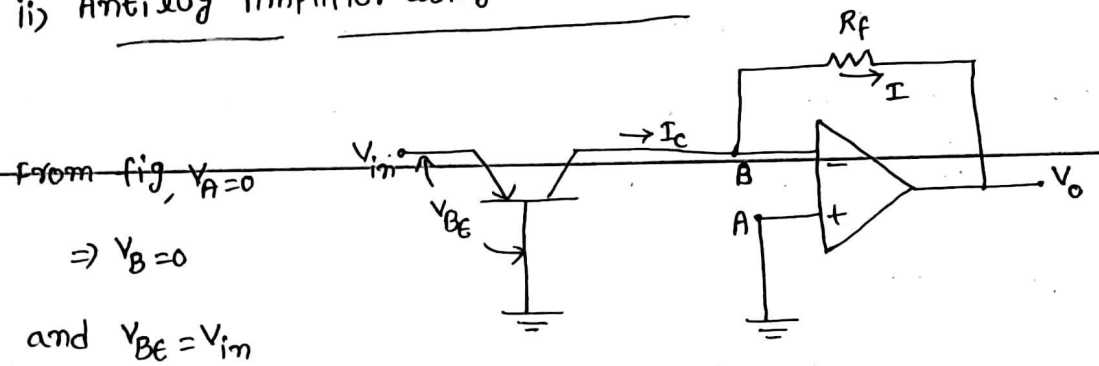
$$\Rightarrow \boxed{V_0 = -I_0 R_f \cdot e^{V_{in}/\eta V_T}} \quad \text{—— ③}$$

Let $V_{ref} = I_0 R_f$, then

$$\boxed{V_0 = -V_{ref}\, e^{V_{in}/\eta V_T}} \quad \text{—④}$$

Thus, the output voltage is proportional to Exponential function of V_{in}. So, the circuit works as Antilog Amplifier.

ii) Antilog Amplifier using transistor :-



From fig, $V_A = 0$

$\Rightarrow V_B = 0$

and $V_{BE} = V_{in}$

w.k.T $I_C = I_S\, e^{V_{BE}/V_T}$

$= I_S\, e^{V_{in}/V_T}$ —⑤ $[\because V_{in} = V_{BE}]$

From fig, $I = I_C = \frac{V_B - V_0}{R_f} = \frac{-V_0}{R_f}$ $[\because V_B = 0]$ —⑥

evaluating eqn ⑤, ⑥

$$-\frac{V_0}{R_f} = I_S\, e^{V_{in}/V_T}$$

$$\Rightarrow V_0 = -I_S R_f\, e^{V_{in}/V_T} \quad \text{—⑦}$$

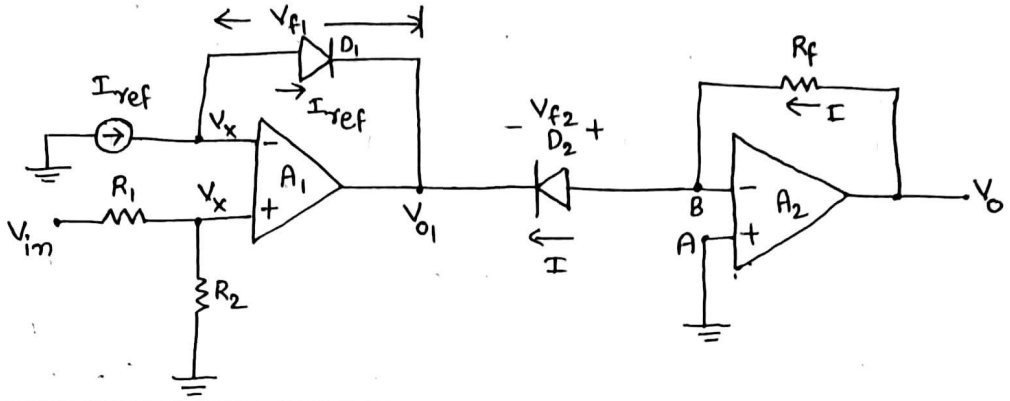
consider $V_{ref} = I_S R_f$, then

$$\boxed{V_0 = -V_{ref}\, e^{V_{in}/V_T}} \quad \text{—⑧}$$

Thus output voltage is proportional to exponential of V_{in} i.e Antilog of V_{in}. Thus circuit works as Antilog Amplifier.

iii) Temperature compensated Antilog Amplifier :-

The Temperature compensation can be provided using diodes.



The OP-Amp A_1, Non-Inverting terminal, Apply voltage divider rule,

$$V_x = \frac{R_2}{R_1+R_2} V_{in} \quad \text{—(9)}$$

From fig, $V_{01} = V_x - V_{f1}$ —(10)

w.k.T $V_{f1} = \eta V_T \ln\left(\frac{I_f}{I_0}\right)$ —(11)

Sub. eq(9), (11) in (10),

$$V_{01} = \frac{R_2}{R_1+R_2} V_{in} - \left[\eta V_T \ln\left(\frac{I_f}{I_0}\right)\right] \quad \text{—(12)}$$

OP-Amp A_2, $V_A = 0$ so, $V_B = 0$

$$\Rightarrow V_{01} = -V_{f2} \quad \text{—(13)}$$

and $V_{f2} = \eta V_T \ln\left(\frac{I_{f2}}{I_0}\right)$ —(14)

where $I_{f2} = I = \frac{V_o - V_B}{R_f} = \frac{V_o}{R_f}$ —(15) $[\because V_B = 0]$

Sub. eq(15) in (14),

$$V_{f2} = \eta V_T \ln\left[\frac{V_o}{R_f I_0}\right] \quad \text{—(16)}$$

from eq (13) $V_{o1} = -V_{f2}$

$$\Rightarrow V_{01} = -\eta V_T \ln\left(\frac{V_o}{I_o R_f}\right) \quad \text{---} (17)$$

equating eq (12), (17)

$$V_{in}\left(\frac{R_2}{R_1+R_2}\right) - \eta V_T \ln\left(\frac{I_{ref}}{I_o}\right) = -\eta V_T \ln\left(\frac{V_o}{I_o R_f}\right) \quad [\because I_f = I_{ref}$$

$$V_{in}\left(\frac{R_2}{R_1+R_2}\right) = \eta V_T \left[\ln\left(\frac{I_{ref}}{I_o}\right) - \ln\left(\frac{V_o}{I_o R_f}\right)\right]$$

$$= \eta V_T \left[\ln(I_{ref}) - \ln(I_o) - \ln\left(\frac{V_o}{R_f}\right) + \ln(I_o)\right]$$

$$= \eta V_T \left[\ln\left(\frac{I_{ref} R_f}{V_o}\right)\right] \quad [\because -\ln\left(\frac{V_o}{R_f}\right) = \ln\left(\frac{R_f}{V_o}\right)$$

$$= -\eta V_T \ln\left(\frac{V_o}{I_{ref} R_f}\right)$$

$$\Rightarrow \ln\left(\frac{V_o}{I_{ref} R_f}\right) = -V_{in}\left(\frac{R_2}{R_1+R_2}\right) \Big/ \eta V_T$$

$$\Rightarrow \boxed{V_o = I_{ref} R_f \ln^{-1}\left[\frac{-V_{in} R_2}{\eta V_T (R_1+R_2)}\right]} \quad \text{---} (18)$$

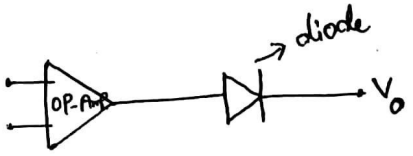
From eq (18), output voltage is proportional to the Antilog ($\ln^{-1}$) of the Input.

Precision rectifiers :-

→ Rectifier is a device which converts A.C to Pulsating D.C

→ The main draw back in rectifier circuit is it does not conduct (or) rectify voltages below 0.7V.

→ In precision rectifiers it can rectify voltages having Amplitude less than 0.7V.

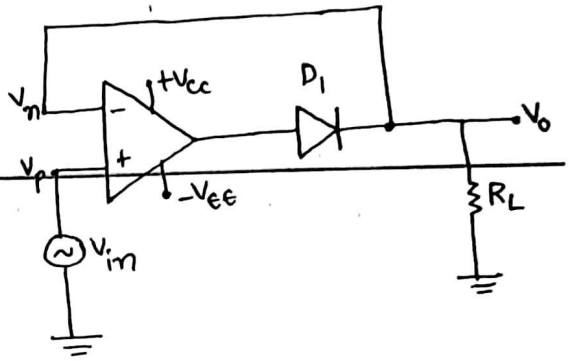


Precision rectifiers are 2 types

1. Precision Half wave rectifier
2. Precision full wave rectifier

1. Precision Half wave rectifier :-

i) Positive Precision half wave rectifier :- (or) Non-Inverting half wave Precision rectif



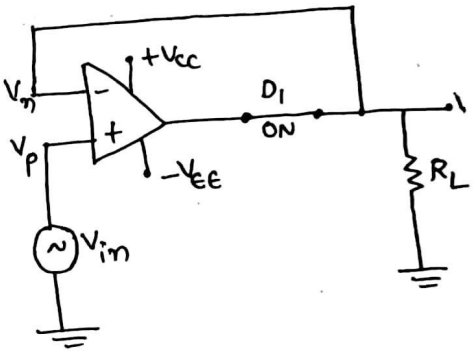
From fig, $V_{in} = V_p$

concept of virtual ground

$$V_n = V_p = V_{in}$$

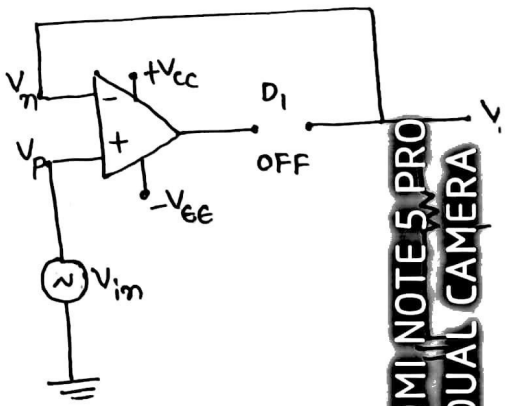
case① $V_{in} > 0V$

In this case, +ve input voltage applied so the diode act as forward bias condition and D_1 becomes short circuit (ON Position) it produces output in the +ve half cycle.

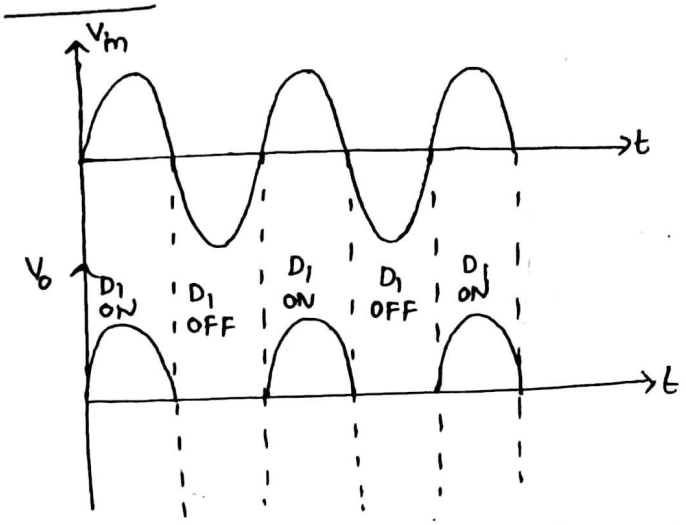


case② $V_{in} < 0V$

In this case -ve Input voltage is applied, diode is in reverse bias condition i.e D_1 becomes open circuit (OFF Position) so it produces no output (zero output) in the -ve half cycle.

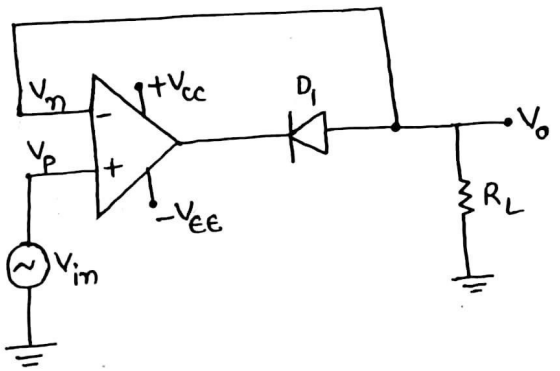


output wave forms:-



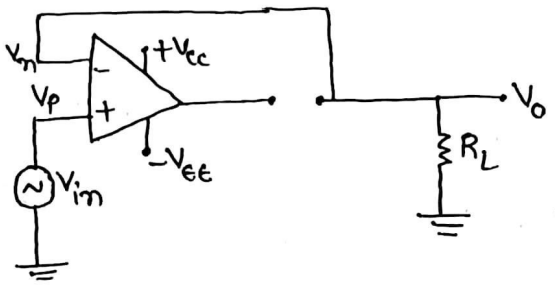
ii) Negative precision half wave rectifier ~~(or) Inverting half wave rectifier~~

case① $V_{in} > 0V$:-



In this case, we are applying +ve Input voltage, so the diode reverse biased making it open.

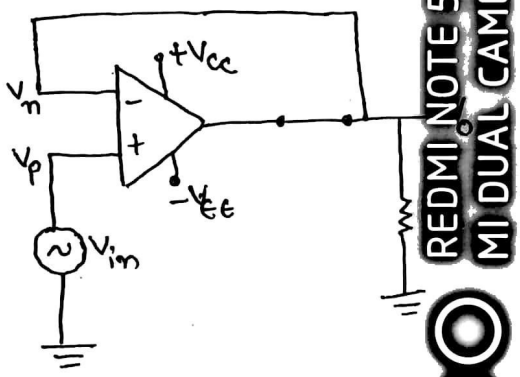
Thus output voltage $V_o = 0V$ so no current pass through R_L.



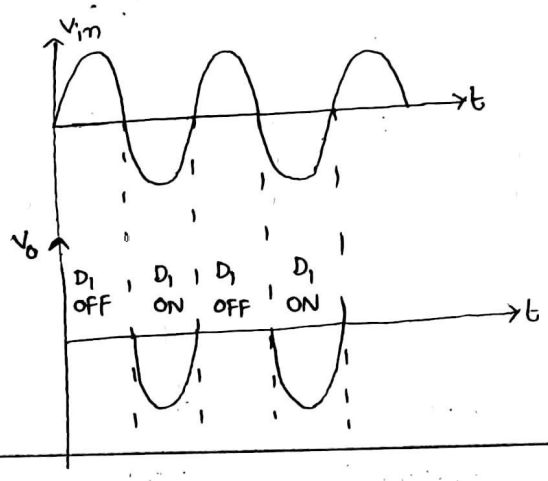
case② $V_{in} < 0V$

In this case, we are applying -Ve Input voltage, so the diode forward biased making it open.

Thus output voltage is same as the Input voltage.



output waveforms :-



2. Precision full wave rectifiers :-

The full wave rectifier circuit accept an A.C signal at the Input, Inverts either -ve (or) +ve half, and delivers both Inverted and Non Inverted halves at the output.

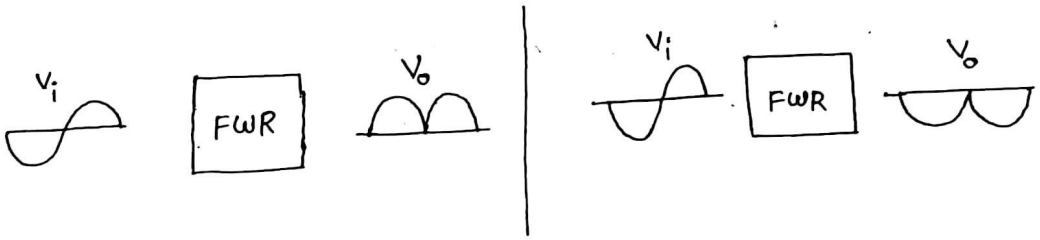
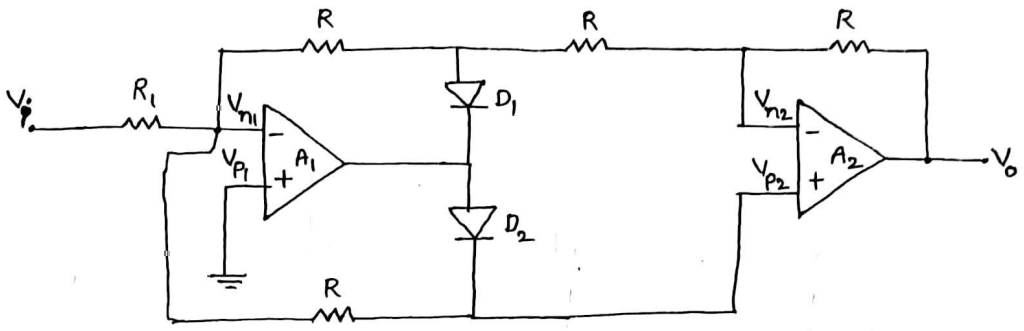


Fig:- +ve and -ve full wave rectifiers

The operation of +ve full wave rectifier is

$$V_o = |V_i| \quad \text{—①}$$

and -ve rectifier as $V_o = -|V_i|$ —②

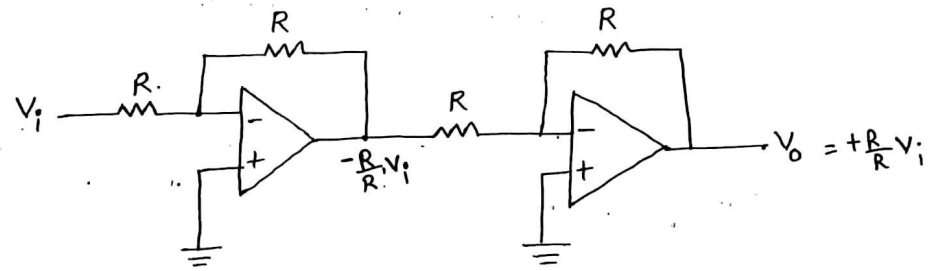


Case ① $V_i > 0V$

Positive Input voltage is applied to input of Inverting termin of OP-Amp A_1 hence output is -Ve voltage.

This -Ve voltage is given to diodes D_1, D_2 hence D_1 is Forward bias and D_2 is reverse bias, so D_1 ON & D_2 OFF.

The equivalent circuit as



From fig,

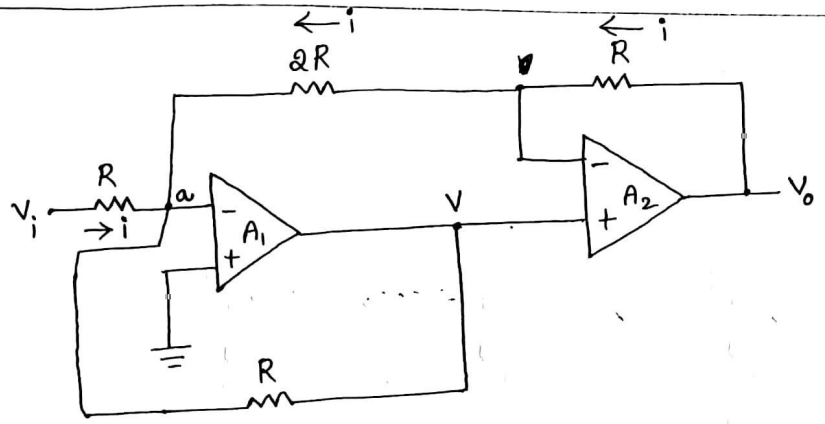
output voltage $V_o = \left(\frac{R}{R}\right) V_i$

$V_o = V_i \Rightarrow \boxed{V_o = +V_i}$

case ② $V_i < 0V$

Apply -Ve voltage output of OP-Amp A_1 has +Ve voltage it makes D_1 reverse bias and D_2 Forward bias.

The equivalent circuit as



Apply KCL at node 'a'

$$\frac{V_i}{R} + \frac{V}{2R} + \frac{V}{R} = 0 \quad \text{—①} \qquad \left[\because i = \frac{V_i}{R} \;\&\; i = \frac{V}{2R},\; i = \frac{V}{R}\right]$$

$$\Rightarrow \frac{V}{2R} + \frac{V}{R} = -\frac{V_i}{R}$$

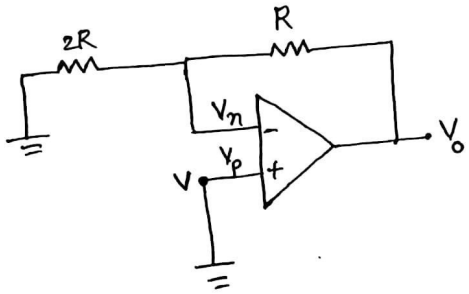
$$\Rightarrow V\left[\frac{1}{2R} + \frac{1}{R}\right] = -\frac{V_i}{R}$$

$$\Rightarrow V\left[\frac{R+2R}{R(2R)}\right] = -\frac{V_i}{R}$$

$$\Rightarrow V\left[\frac{3R}{2R \cdot R}\right] = -\frac{V_i}{R}$$

$$\Rightarrow V = -\frac{2}{3} V_i \quad \text{—②}$$

consider equivalent circuit,



From fig,

$$V_o = \left(1 + \frac{R}{2R}\right) V$$

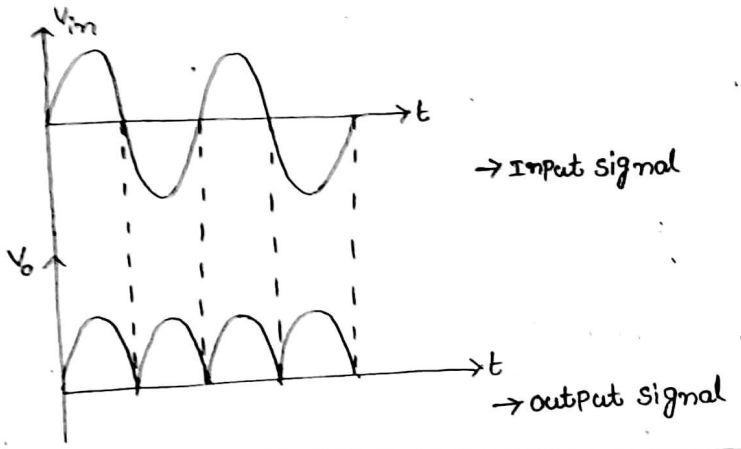
$$= \left(\frac{2R+R}{2R}\right) V$$

$$= \frac{3R}{2R} V = \frac{3}{2} V \quad \text{—③}$$

sub. eq ② in ③

$$\Rightarrow V_o = \frac{3}{2}\left[\frac{-2}{3}\right] V_i \Rightarrow \boxed{V_o = -V_i}$$

output wave forms :-



G. Venkata Hanuma
Asst. Prof

4. Active filters & Analog multipliers & modulators

Filter → It is a circuit that designed to pass a specified band of frequencies while attenuating all the signals outside that band.

Filters are classified into 2 types

1. Passive filter → contain passive elements resistor, Inductor, capacitor
2. Active filter
   ↳ contains Active elements such as OP-Amps, transistors

Advantages of Active filters :-

1. Reduction of size and weight
2. Low cost
3. Due to availability of modern ICs, Variety of cheaper OP-Amps are available.
4. The OP-Amp gain can be easily controlled in closed loop fashion.
5. Due to flexibility in gain and frequency adjustments, active filters can be easily tuned.
6. The OP-Amp has high Input Impedance, low output Impedance. hence the active filters using OP-Amps

7. The Inductors are absent in the active filters. hence the modern Active filters are more economical.

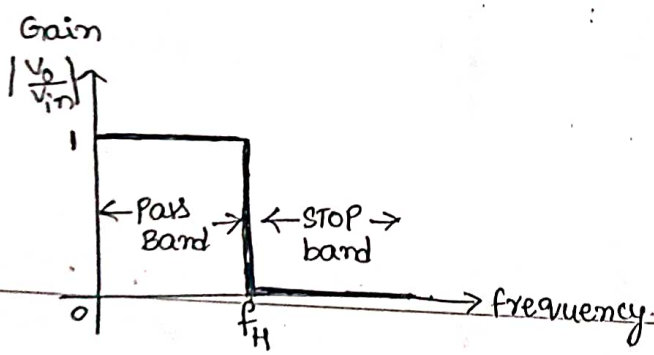
8. Active filters can be realized under no.of class of functions such as Butterworth, chebyshev, Thomson etc..

9. Active filters Provide Voltage gain.

10. The design Procedure is simpler than that of passive filters.

Frequency response characteristics of filters :-

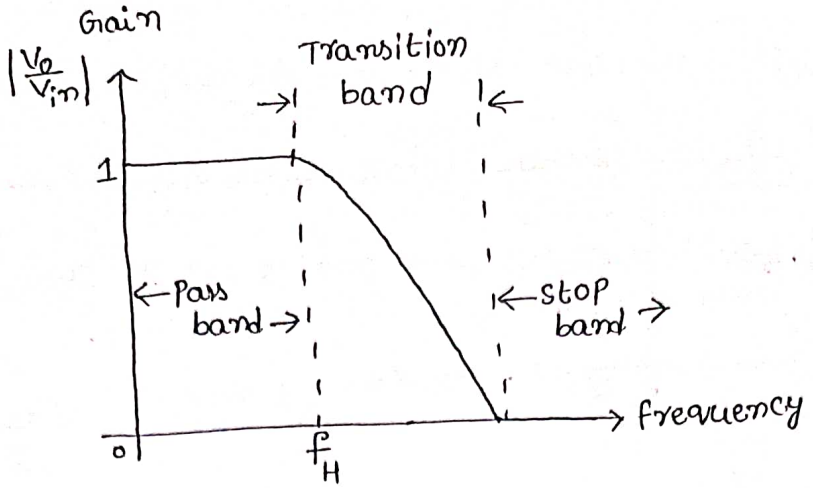
1. Low Pass filter (LPF) :-



a) Ideal LPF

The circuit allows the range of frequencies from 0 to f_H is called "Pass band" and range of frequencies beyond f_H is completely attenuated is called "stop band".

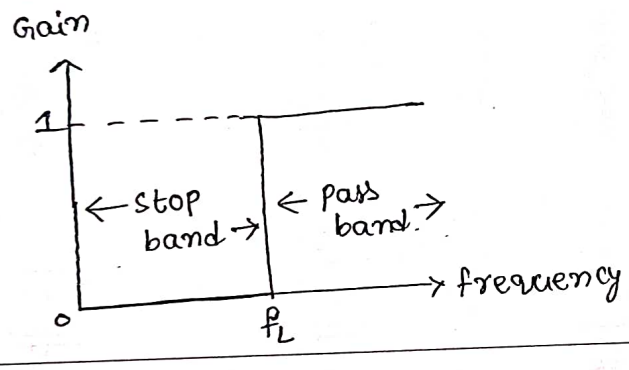
Practically, gain of filter decreases as frequency increases and $f = f_H$, gain is down by 3dB after f_H, it decreases at higher rate. After end of transition band, gain becomes zero.



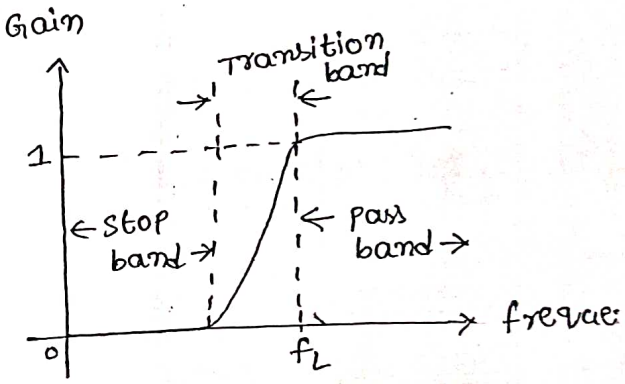
b) Practical

2. High pass filter (HPF) :-

It allows high frequencies and reject (attenuates) Low frequencies.



a) Ideal

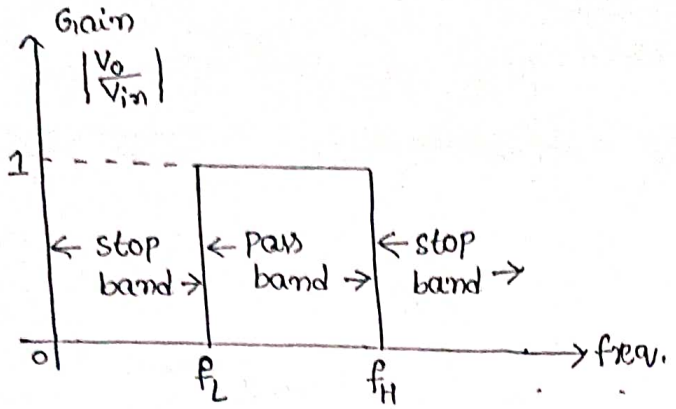


b) Practical

The range of frequency $0<f<f_L$ is the stop band where f is the operating frequency while the range of frequency $f>f_L$ is the pass band.

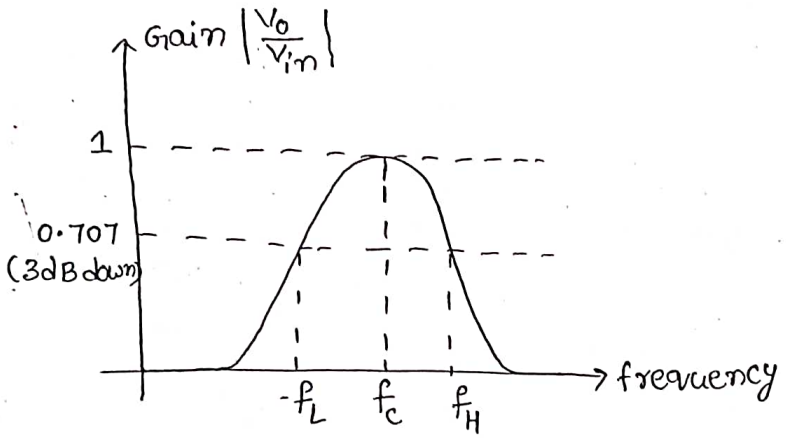
3. Band pass filter (BPF) :-

It allows only certain band of frequencies (Passband) and attenuates remaining all frequencies (stop band



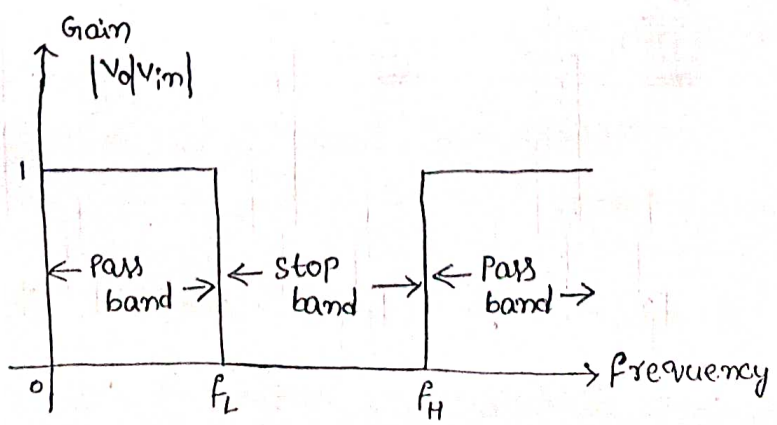
a) Ideal

The range of frequency $0<f<f_L$ and range of frequency $f_H<f<\infty$ are 2 stop bands while range $f_L<f<f_H$ is passband.



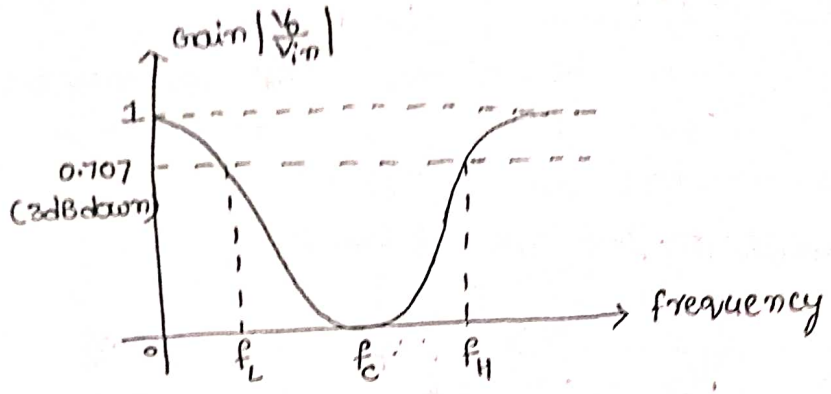
b) Practical

4. Band reject filter :- It also called Band elimination filter (or) Band stop filter.



There are 2 pass bands while one stop band. The stop band between 2 frequencies f_L, f_H. The two ranges $0 < f < f_L$ and $f_H < f < \infty$ are two pass bands.

The frequency response characteristics of band elimination filter is shown in fig.



b) Practical

→ At frequency $f = f_c$, practical characteristics shows a notch and hence filter is called "Notch filter."

All Pass filter:-

All pass filter passes all frequencies but it produces phase shift between Input and output.

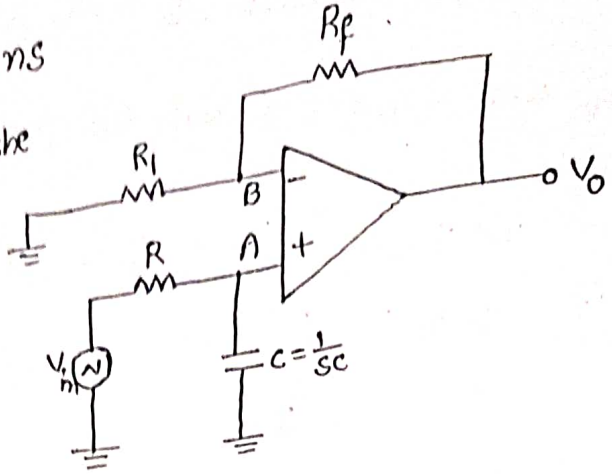
The output and Input voltages are equal in Amplitude for all frequencies but with phase shift between the two.

Applications:- Audio applications Include filter banks.

First order Low Pass Butterworth filter :-

The No. of RC sections used in circuit gives the order of filter.

Here only one RC section used for 1st order LPF.



From fig,

Potential divider rule at node 'A',

$$V_A = \frac{-jX_C}{R-jX_C} \cdot V_{in} \qquad \text{——} (1)$$

we know that $X_C = \frac{1}{2\pi fc}$

$$V_A = \frac{-j\left(\frac{1}{2\pi fc}\right)}{R-j\left(\frac{1}{2\pi fc}\right)} \cdot V_{in}$$

$$= \frac{-j}{R(2\pi fc)-j} \cdot V_{in}$$

$$= \frac{-j}{-j\left(1-\frac{2\pi fRc}{j}\right)} \cdot V_{in} = \frac{1}{1-\frac{2\pi fRc}{j}} \cdot V_{in}$$

But $-j = \frac{1}{j}$

$$\Rightarrow V_A = \frac{V_{in}}{1+j2\pi fRc} \qquad \text{——} (2)$$

Input is given to Non-Inverting terminal,

we know that $A = 1 + \frac{R_f}{R_1}$

$$\frac{V_o}{V_A} = 1 + \frac{R_f}{R_1}$$

$$\Rightarrow V_o = \left(1 + \frac{R_f}{R_1}\right) V_A \quad \text{—③}$$

Substitute eq ② in ③

$$V_o = \left(1 + \frac{R_f}{R_1}\right)\left(\frac{V_{in}}{1 + j2\pi fRC}\right)$$

$$\Rightarrow \frac{V_o}{V_{in}} = \left(1 + \frac{R_f}{R_1}\right) \cdot \frac{1}{1 + j(f/f_H)} \qquad \left[\because f_H = \frac{1}{2\pi RC}\right]$$

$$\Rightarrow \boxed{\frac{V_o}{V_{in}} = \frac{A_F}{1 + j(f/f_H)}} \quad \text{—④} \qquad \left[\because A_F = 1 + \frac{R_f}{R_1}\right]$$

where, $A_F \rightarrow$ Gain of Filter in Passband

$f_H \rightarrow$ High cut off frequency of filter (or) corner (or) Break frequency

$f \rightarrow$ frequency

eq ④ expressed in Polar form as,

$$\left|\frac{V_o}{V_{in}}\right| = \frac{A_F}{\sqrt{1 + (f/f_H)^2}} \quad \text{—⑤}$$

and $\phi = -\tan^{-1}\left(\frac{f}{f_H}\right)$ —⑥

case ① :- At $f < f_H$,

$\left|\frac{V_o}{V_{in}}\right| \simeq A_F$ i.e constant

case 2 :- At $f = f_H$,

$$\left|\frac{V_o}{V_{in}}\right| = \frac{A_F}{\sqrt{1+(1)^2}} = \frac{A_F}{\sqrt{2}} = 0.707\,A_F$$

i.e 3dB down to the level o

case 3 :- At $f > f_H$,

$$\left|\frac{V_o}{V_{in}}\right| < A_F$$

characteristics :-

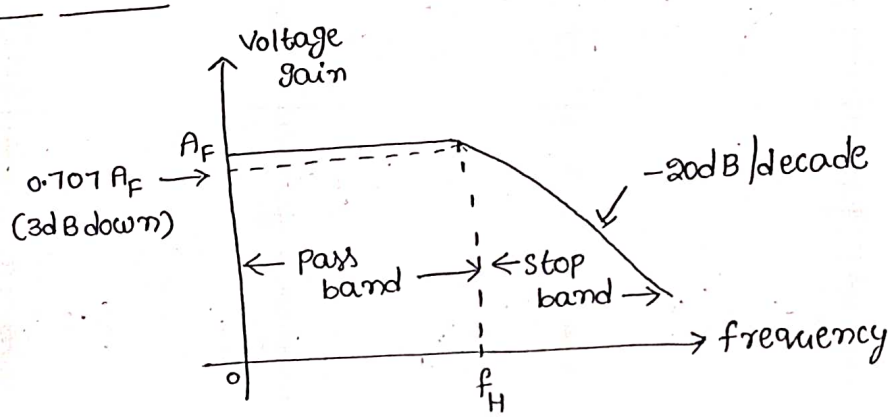


Fig :- frequency response

→ At $f = f_H$, gain reduces to $0.707\,A_F$ i.e 3dB down from A_F.

→ As frequency Increases than f_H, gain decreases at a rate of 20dB/decade.

→ The frequency f_H is called cut-off frequency, break frequer -3dB frequency (or) corner frequency.

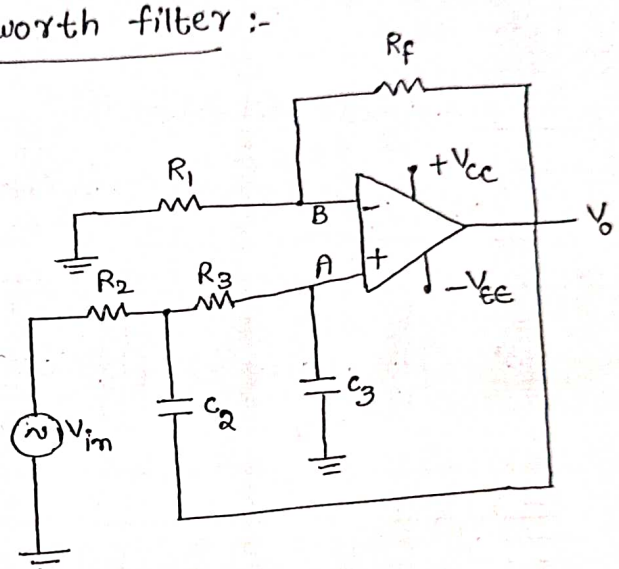
Design steps:-

1. choose the cut-off frequency f_H i.e $f_H = \frac{1}{2\pi RC}$
2. choose capacitor C=0.001 and 1MF. Generally it selected as 1MF
3. The resistances R_f, R_1 can be selected depending on gain in pass band.

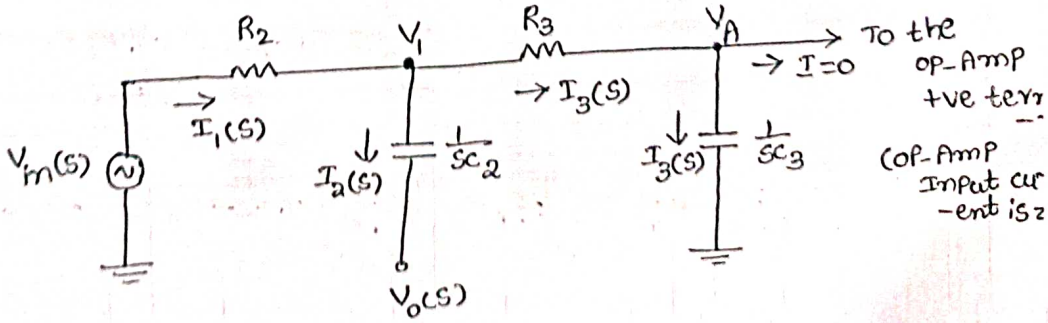
$$A_F = 1 + \frac{R_f}{R_1}$$

Second order lowpass Butterworth filter :-

* 1st order filter can be converted to 2nd order type by using an additional RC Network.



Analysis:- The Input RC Network can be represented in Laplace-domain as shown in fig.



Apply KCL,

$$I_1 = I_2 + I_3 \quad \text{—①}$$

$$\Rightarrow \frac{V_{in}-V_1}{R_2} = \frac{V_1-V_o}{1/sC_2} + \frac{V_1-V_A}{R_3} \quad \text{—(2)}$$

using potential divider rule, at V_A

$$V_A = \left[\frac{\frac{1}{sC_3}}{R_3+\frac{1}{sC_3}}\right] V_1 \quad \text{—(3)}$$

$$V_A = \frac{V_1}{1+R_3sC_3} \quad \text{—(4)}$$

$$\Rightarrow V_1 = V_A(1+R_3sC_3) \quad \text{—(5)}$$

substitute eq (5) in (2),

$$\frac{V_{in}-V_A(1+R_3sC_3)}{R_2} = \frac{V_A(1+sR_3C_3)-V_o}{1/sC_2} + \frac{V_A(1+R_3sC_3)-V_A}{R_3}$$

$$\Rightarrow \frac{V_{in}}{R_2} - \frac{V_A(1+sR_3C_3)}{R_2} = \frac{V_A(1+sR_3C_3)}{1/sC_2} - \frac{V_o}{1/sC_2} + \frac{V_A}{R_3}(1+sR_3C_3) - \frac{V_A}{R_3}$$

$$\Rightarrow \frac{V_{in}}{R_2} + \frac{V_o}{1/sC_2} = \frac{V_A}{R_2}(1+sR_3C_3) + \frac{V_A}{1/sC_2}[1+sR_3C_3] + \frac{V_A}{R_3}(1+sR_3C_3) - \frac{V_A}{R_3}$$

$$\Rightarrow \frac{V_{in}}{R_2} + V_o(sC_2) = V_A\left[\frac{1+sR_3C_3}{R_2} + \frac{1+sR_3C_3}{1/sC_2} + \frac{1+sR_3C_3}{R_3} - \frac{1}{R_3}\right]$$

$$= V_A\left[\frac{R_3(1+sR_3C_3)+R_2R_3sC_2(1+sR_3C_3)+R_2(1+sR_3C_3)-R_2}{R_2R_3}\right]$$

$$\Rightarrow \left(\frac{V_{in}}{R_2} + V_o sC_2\right) R_2R_3 = V_A\left[(1+sR_3C_3)\left[R_3+R_2R_3sC_2+R_2\right)-R_2\right]$$

$$\Rightarrow V_{in}R_3 + V_o sR_2R_3C_2 = V_A\left[(1+sR_3C_3)(R_3+R_2R_3sC_2+R_2)-R_2\right]$$

$$V_A = \frac{V_{in}R_3 + V_o S R_2 R_3 C_2}{[(1+SR_3C_3)(R_3+R_2R_3SC_2+R_2)-R_2]} \quad \text{---(6)}$$

OP-AMP In Non-Inverting configuration,

w.k.t $\frac{V_o}{V_A} = 1 + \frac{R_F}{R_1}$ $\left[\because A_F = 1+\frac{R_F}{R_1}, \frac{V_o}{V_A} = 1+\frac{R_F}{R_1}\right]$

$$\Rightarrow \frac{V_o}{V_A} = A_F \Rightarrow V_o = A_F \cdot V_A$$

$$V_o = A_F \left[\frac{R_3 V_{in} + V_o S R_2 R_3 C_2}{(1+SR_3C_3)(R_3+R_2R_3SC_2+R_2)-R_2}\right]$$

$$\Rightarrow V_o = \frac{A_F R_3 V_{in}}{(1+SR_3C_3)(R_3+R_2R_3SC_2+R_2)-R_2} + \frac{A_F V_o S R_2 R_3 C_2}{(1+SR_3C_3)(R_3+R_2R_3SC_2+R_2)-R_2}$$

$$\Rightarrow V_o - \frac{A_F V_o S R_2 R_3 C_2}{(1+SR_3C_3)(R_3+R_2R_3SC_2+R_2)-R_2} = \frac{A_F R_3 V_{in}}{(1+SR_3C_3)(R_3+R_2R_3SC_2+R_2)-R_2}$$

$$\Rightarrow V_o\left[1 - \frac{A_F S R_2 R_3 C_2}{(1+SR_3C_3)(R_3+R_2R_3SC_2+R_2)-R_2}\right] = \frac{A_F R_3 V_{in}}{(1+SR_3C_3)(R_3+R_2R_3SC_2+R_2)-R_2}$$

$$\Rightarrow V_o\left[\frac{(1+SR_3C_3)(R_3+R_2R_3SC_2+R_2)-R_2-A_F SR_2R_3C_2}{(1+SR_3C_3)(R_3+R_2R_3SC_2+R_2)-R_2}\right]$$

$$= \frac{A_F R_3 V_{in}}{(1+SR_3C_3)(R_3+R_2R_3SC_2+R_2)-R_2}$$

$$\Rightarrow A_F R_3 V_{in} = V_o\left[(1+SR_3C_3)(R_3+R_2R_3SC_2+R_2) - R_2 - SR_2R_3C_2A_F\right] \quad \text{---(6}$$

$$\Rightarrow \frac{V_o}{V_{in}} = \frac{A_F R_3}{(1+SR_3C_3)(R_3+R_2R_3SC_2+R_2)-R_2-SR_3R_2C_2A_F}$$

$$\Rightarrow \frac{V_0}{V_{in}} = \frac{A_F}{s^2 + \frac{(R_3C_3 + R_2C_3 + R_2C_2 - A_F R_2 C_2)s}{R_2R_3C_2C_3} + \frac{1}{R_2R_3C_2C_3}}$$

The order of 's' in the above expression is two, the filter is called "2nd order filter"

The standard form of the transfer function of any 2nd order system is

$$\frac{V_0(s)}{V_{in}(s)} = \frac{A}{s^2 + 2\xi\omega_n s + \omega_n^2} \quad \text{— (9)}$$

compare eq⑧, ⑨

$$\omega_n^2 = \frac{1}{R_2R_3C_2C_3}$$

In case of filters, frequency is cut-off frequency, ω_H

$$\Rightarrow \omega_H^2 = \frac{1}{R_2R_3C_2C_3}$$

$$\Rightarrow (2\pi f_H)^2 = \frac{1}{R_2R_3C_2C_3}$$

$$\Rightarrow f_H^2 = \frac{1}{4\pi^2 R_2R_3C_2C_3}$$

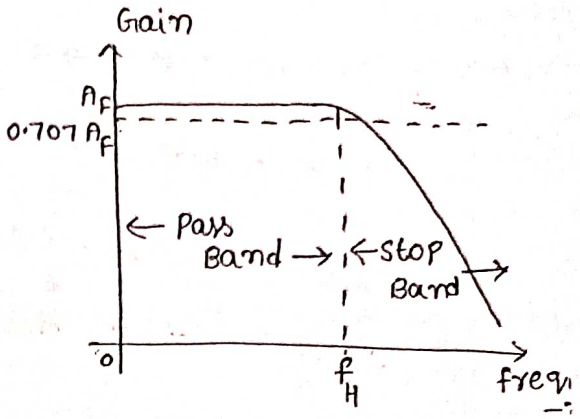
$$\Rightarrow \boxed{f_H = \frac{1}{2\pi\sqrt{R_2R_3C_2C_3}}} \quad \text{— (10)}$$

In Polar form, $\left|\frac{V_0}{V_{in}}\right| = \frac{A_F}{\sqrt{1 + \left(\frac{f}{f_H}\right)^4}}$ — (11)

The frequency response is shown in fig.

→ The cut-off frequency f_H, gain is $0.707A_F$ i.e 3dB down from its 0Hz level.

→ After f_H, gain rolls off at a rate of 40 dB/decade.



Design steps :-

To design 2nd order low pass Butterworth filter having

1. choose cut-off frequency f_H.
2. Design can be simplified by selecting $R_2=R_3=R$ and $C_2=C_3=C$ choose 'C' value less than (or) equal to 1MF
3. calculate value of 'R' from equation,

$$f_H = \frac{1}{2\pi\sqrt{R_2R_3C_2C_3}} = \frac{1}{2\pi RC}$$

4. AS $R_2=R_3=R$ and $C_2=C_3=C$, pass band voltage gain $A_F = 1+\frac{R_f}{R_1}$ of the 2nd order filter equal to 1.586

Note :-

To ensure Butterworth response, gain A_F is 1.586

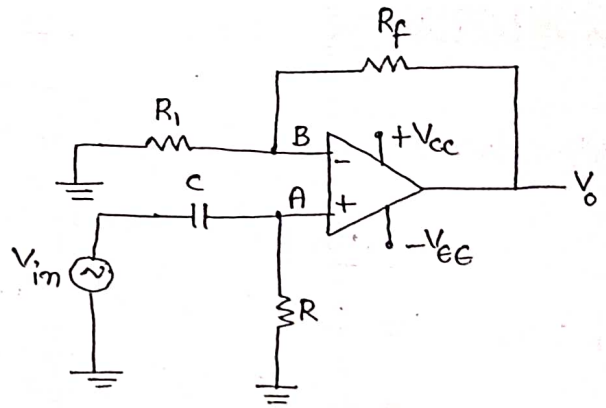
i.e $1.586 = 1+\frac{R_f}{R_1}$

$$\Rightarrow \boxed{R_f = 0.586R_1}$$

First order High pass Butterworth filter :-

→ A High pass filter is a circuit that attenuates all signals below specified cut-off frequency f_L.

→ By Inter changing the elements R and C in a 1st order Low Pass filter circuit it forms High pass filter circuit.



From fig,

By using voltage divider rule at node 'A'

$$V_A = \left[\frac{R}{R - jX_C}\right] V_{in} \quad \text{—①}$$

$$= \left[\frac{R}{-jX_C\left[\frac{R}{-jX_C} + 1\right]}\right] V_{in}$$

$$= \left[\frac{\left(\frac{-R}{jX_C}\right)}{\left(\frac{-R}{jX_C}\right) + 1}\right] V_{in} \quad \text{——②}$$

$$\Rightarrow V_A = \left[\frac{j2\pi f RC}{j2\pi f RC + 1}\right] V_{in} \quad \text{——③}$$

$$\left[\because -\frac{1}{jX_C} = \frac{j}{X_C} = \frac{j}{\cancel{2\pi f}\left(\frac{1}{2\pi fC}\right)} = j2\pi fC\right]$$

consider $f_L = \frac{1}{2\pi RC}$ → Low cut-off frequency

$$\Rightarrow V_A = \left[\frac{j\left(\frac{f}{f_L}\right)}{j\left(f/f_L\right) + 1}\right] V_{in} \quad \text{——④}$$

The op-Amp in Non-Inverting configuration,

$$\frac{V_o}{V_A} = \left(1 + \frac{R_f}{R_1}\right)$$

$$A_F = \left(1 + \frac{R_f}{R_1}\right)$$

$$\Rightarrow V_o = V_A \left[1 + \frac{R_f}{R_1}\right] \quad \text{——} (5) \Rightarrow V_o = V_A \cdot A_F \quad \text{——} (5)$$

substitute eqv (4) in (5)

$$\Rightarrow V_o = A_F \cdot \left[\frac{j(f/f_L)}{j(f/f_L)+1}\right] V_{in}$$

$$\Rightarrow \frac{V_o}{V_{in}} = A_F \left[\frac{j(f/f_L)}{j(f/f_L)+1}\right] \quad \text{——} (6)$$

magnitude is given by,

$$\left|\frac{V_o}{V_{in}}\right| = \frac{A_F (f/f_L)}{\sqrt{1+(f/f_L)^2}} \quad \text{——} (7)$$

eqv (7), describes the behaviour of high pass filter.

1. At low frequencies, $f < f_L$

$$\left|\frac{V_o}{V_{in}}\right| < A_F$$

2. At $f = f_L$, $\left|\frac{V_o}{V_{in}}\right| = 0.707 A_F$ i.e 3dB down from the level of

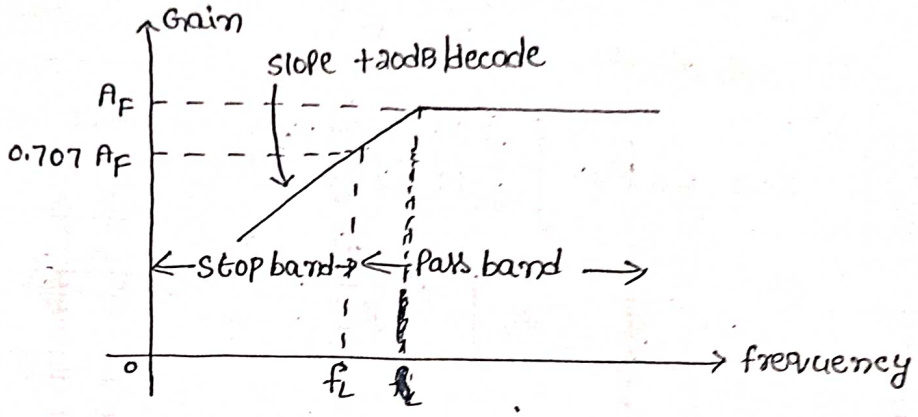
3. At $f > f_L$, i.e high frequencies,

$$\left|\frac{V_o}{V_{in}}\right| \cong A_F$$ i.e constant.

→ The circuit act as a high pass filter with a pass band gain as,

→ At $f < f_L$, gain increases till $f = f_L$ at a rate of +20dB/decade. Hence slope of frequency response in stop band is +20dB/decade for 1st order high pass filter.

Frequency response is shown in fig.



Second order High Pass Butterworth filter :-

This filter can be obtained by interchanging positions of R and C in 2nd order Low Pass Butterworth filter.

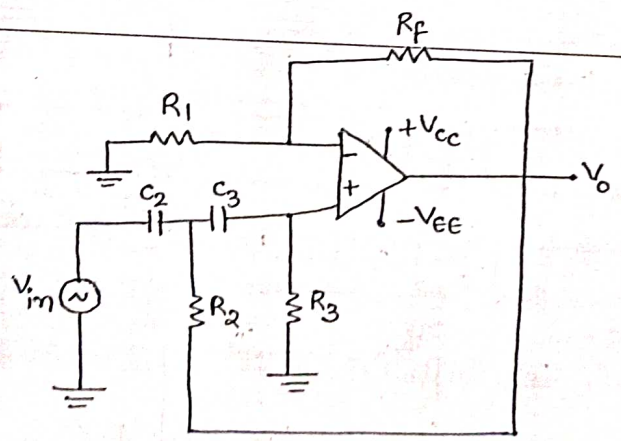


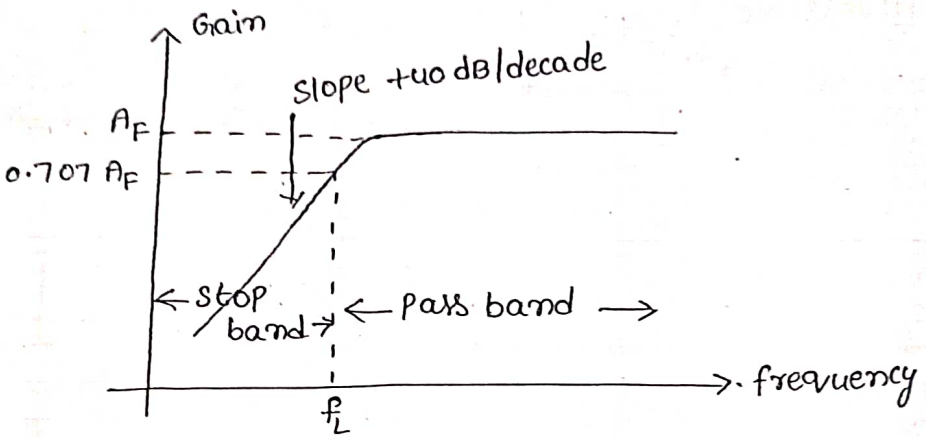
Fig:- second order high pass Butterworth filter

The Analysis, design and procedures for this filter is exactly same as that of 2nd order low pass Butterworth filter.

i.e $\left|\frac{V_o}{V_{in}}\right| = \frac{A_F}{\sqrt{1+(f_L/f)^4}}$

$f_L = \frac{1}{2\pi\sqrt{R_2R_3C_2C_3}}$

The frequency response of this filter as shown in fig.

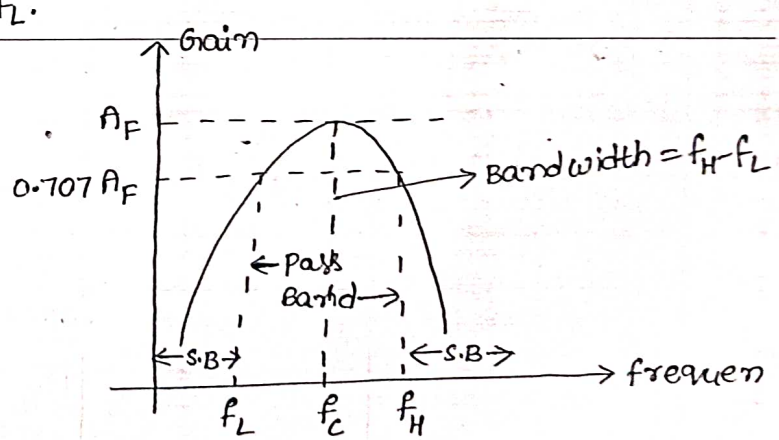


Band Pass filters:-

It allows one particular band of frequencies to pass. Thus, pass band in between f_H and f_L.

→ Pass band which is between f_H and f_L is called Bandwidth.

$B.\omega = f_H - f_L$



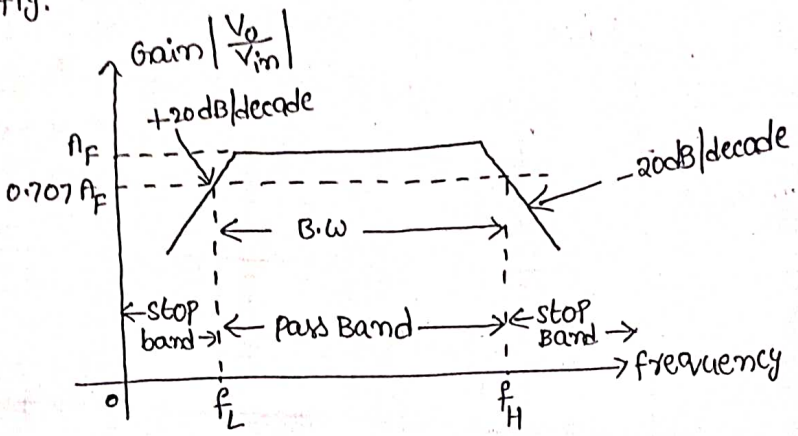
→ There are 2 types of Band Pass filters based on figure of merit (or) Quality factor (Q).

1. wide Band pass filter (Q<10)

2. Narrow Band pass filter. (Q>10)

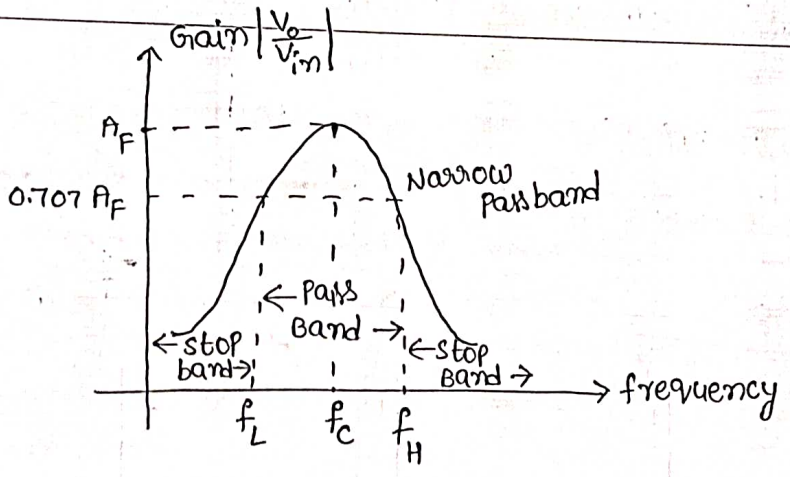
1. wide band pass filter :-

For Q<10, the band pass filter is called wide band pass filter. In this type, the Band width is more. The response is shown in fig.



2. Narrow Band pass filter :-

For Q>10, the band pass filter is called narrow band pass filter. In this type, Band width is very small. The response is shown in fig.



The gain roll off for $f<f_L$ is +20dB/decade and $f>f_H$ is -20dB/decade.

and center frequency $\boxed{f_C = \sqrt{f_L f_H}}$

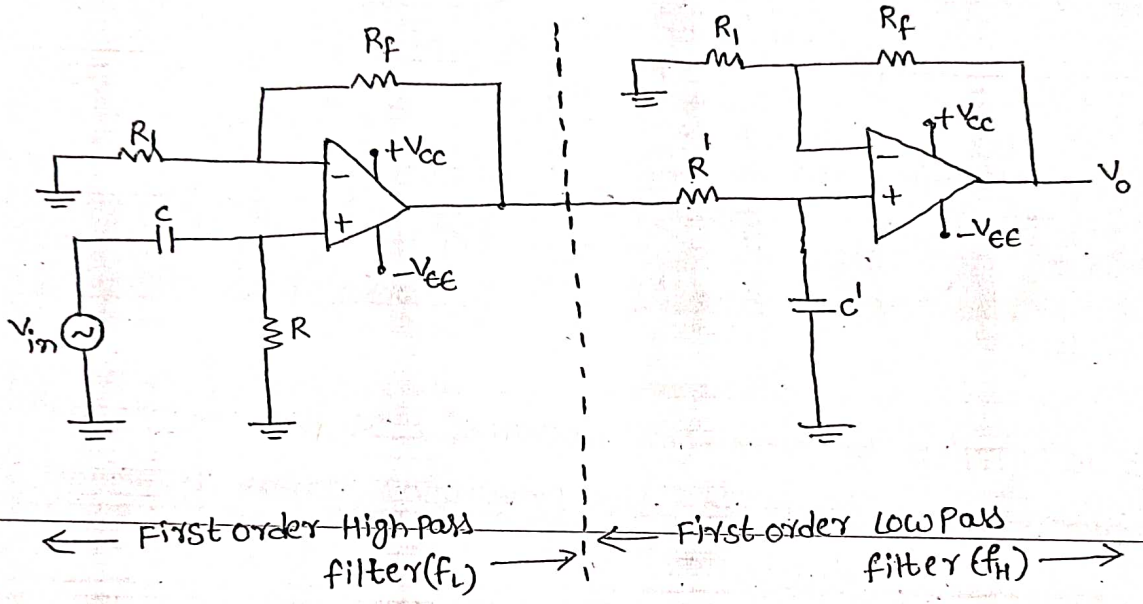
The relation ship between Q and Bandwidth is

$$Q = \frac{f_c}{BW} = \frac{f_c}{f_H - f_L}$$

wide band pass filter:-

wide band pass filter is formed by cascading high pass filter and low pass filter.

→ If HPF and LPF are 1st order, then band pass filter will have a roll-off rate of -20dB/decade.



For wide band pass response, f_H must be greater than f_L.

For Low pass → $\left|\frac{V_o}{V_{in}}\right| = \frac{A_F}{\sqrt{1+(f/f_H)^{2n}}}$

For High pass → $\left|\frac{V_o}{V_{in}}\right| = \frac{A_F (f/f_L)}{\sqrt{1+(f/f_L)^{2n}}}$

over all gain is Product of 2 gains.

$$\left|\frac{V_o}{V_{in}}\right| = \frac{A_{FT}\,(f/f_L)}{\sqrt{(1+f/f_H)^2\,(1+f/f_L)^2}}$$

where A_{FT} → Total pass band Gain

i.e A_{FT} = Gain of HPF × Gain of LPF.

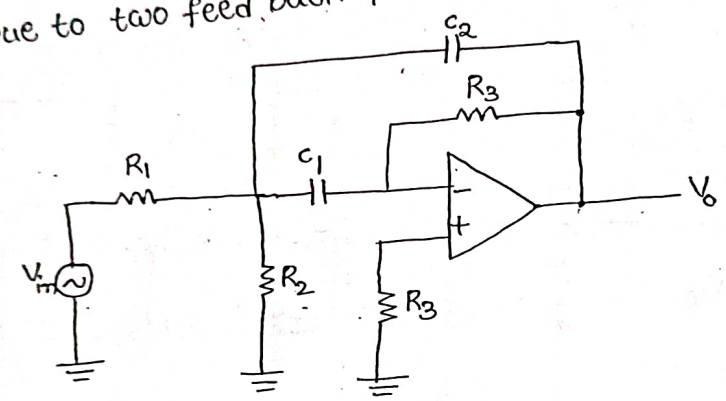
Narrow Band Pass filter :-

The Narrow band pass filter uses only one op-Amp against two by wide band filter.

It has

i) 2 feed back paths ii) op-Amp in Inverting configuration

Due to two feed back paths it also called "multiple feedback filter".



→ Input is applied to Inverting terminal, so it is in Inverting configuration. R_3 connected to Non-Inverting Input terminal is offset compensating resistance.

→ Important parameters are f_L, f_H, center frequency f_c, gain at center frequency A_F, Quality factor Q.

For simplifying calculations, choose $C_1 = C_2 = C$

$$R_1 = \frac{Q}{2\pi f_c C A_F} \quad \text{—— ①}$$

$$R_2 = \frac{Q}{2\pi f_c C (2Q^2 - A_F)} \quad \text{—— ②}$$

$$R_3 = \frac{Q}{\pi f_c C} \quad \text{—— ③}$$

and $A_F = \frac{R_3}{2R_1}$ = Gain at f_c —— (4)

Gain A_F must satisfy the equation, $A_F < 2Q^2$ —(5)

changing the centre frequency f_c :-

Let f_c → original frequency

f_c' → New centre frequency

The new centre frequency can be achieved by changing resistance R_2.

The new value of resistance is

$$R_2' = R_2 \left(\frac{f_c}{f_c'}\right)^2 \quad \text{——(6)}$$

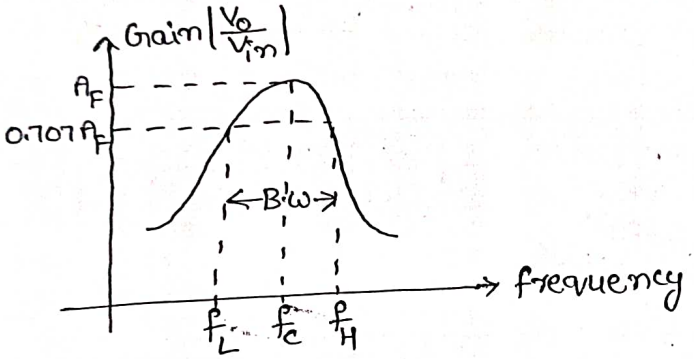


Fig:- Frequency response

* Advantage :- f_c can be changed with out changing gain A_F (or) Band width.

Band Elimination filter :-

It also called "Band stop filter" (or) "Band reject filter

→ This operation is exactly opposite to Band Pass filter.

→ It contains 2 pass bands and 1 stop band.

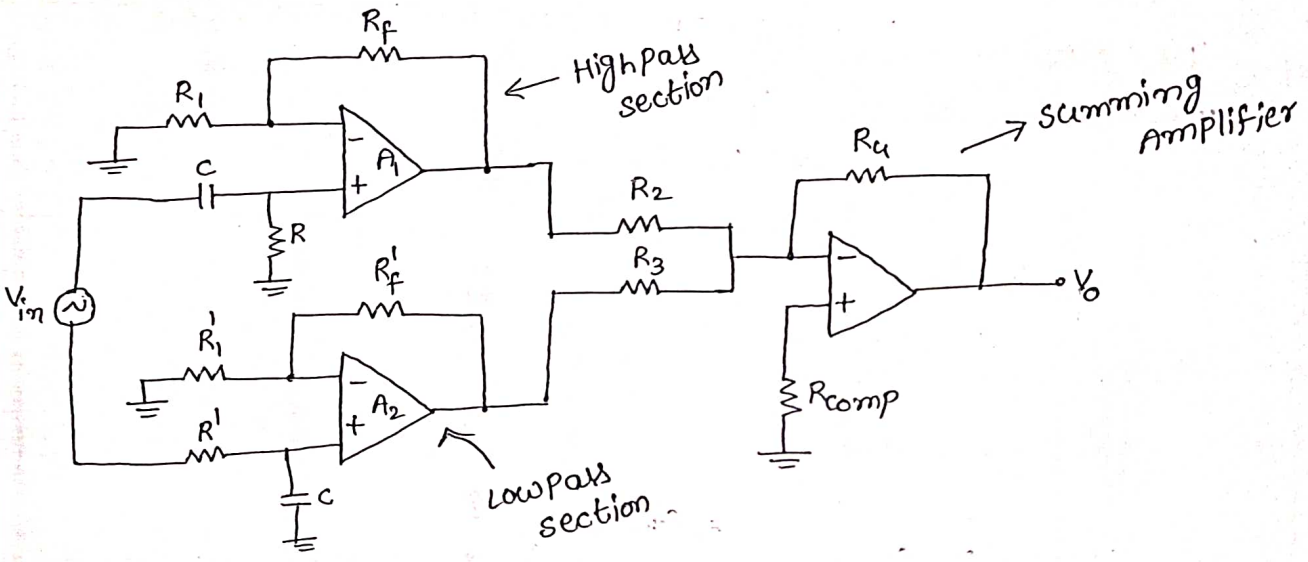
→ A Band of frequencies is attenuated by this filter hence name called as "Band Elimination filter".

→ This filter again divided into 2 types

1. wide band reject filter
2. Narrow band reject filter

1. wide band reject filter :-

Similar to wide band pass filter, it also consists of high pass and Low pass filters, additionally it contains summing Amplifier.



It has 2 conditions

i) The Low cut-off frequency, f_L of high pass filter must be greater than high cut-off frequency, f_H of Low pass filter.

ii) Pass band gain of both high pass and Low pass sections must be equal.

The gain of summing Amplifier can be set to 1 for simplicity

$$R_2 = R_3 = R_4 = R \quad \text{—①}$$

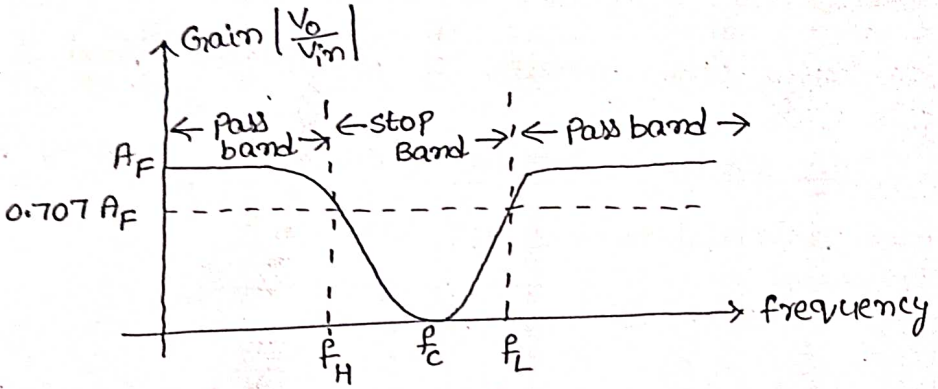
Here, $R_{comp} = R_2 \| R_3 \| R_4 = \frac{R}{3}$ —— ②

Both high pass and low pass sections provide attenuation in stopband between f_H and f_L.

For $f < f_H$, transmission is due to low pass section, while for $f > f_L$, transmission is due to high pass section.

centre frequency, $f_c = \sqrt{f_H f_L}$

The frequency response is shown in fig.



2. Narrow band reject filter (Notch filter) :-

The Application of Notch filter is the rejection of a single frequency, such as 50Hz Power line frequency hum.

→ It is used in Biomedical Instrumentation and also blanking of control tones for telephone lines.

→ By using this filter, particular unwanted frequency can be eliminated.

→ It also called as Twin T Network.

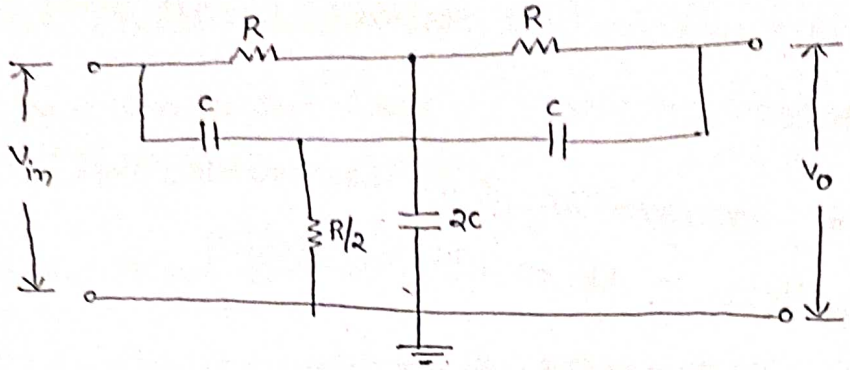


Fig:- Twin T Network

It consists of 2 T Networks. one consists of 2 resistors and a capacitor while other consists of 2 capacitors and 1 resistor.

The Notch out frequency is the frequency at which maximum attenuation occurs.

It given by $f_N = \frac{1}{2\pi RC}$

The value of Q i.e figure of merit for the Passive Network is very low, hence an active Notch filter which uses twin T Network is Preferred in Practice.

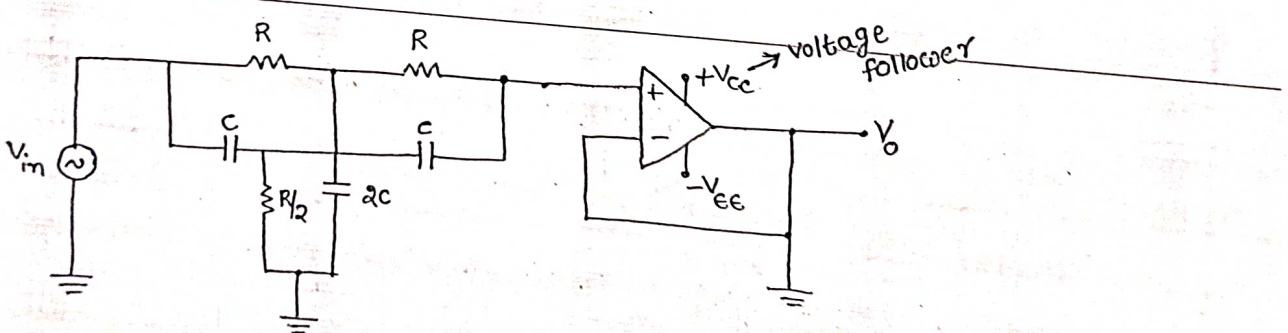
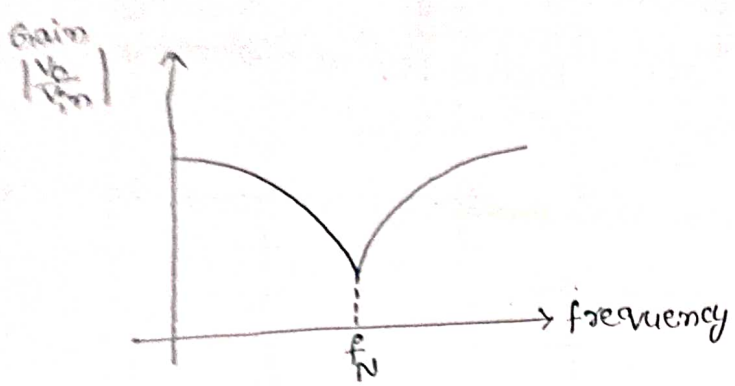


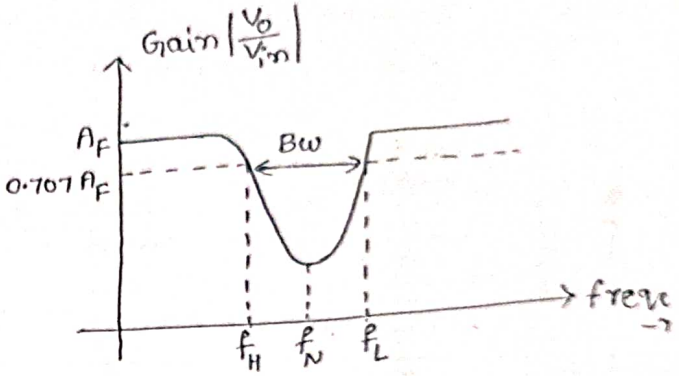
Fig:- Active Notch filter

To design a Notch filter, to eliminate specific Notch frequency f_N, choose capacitor 'C' less than (or) equal to 1MF. Then, calculate 'R' using $f_N = \frac{1}{2\pi RC}$ expression.

The frequency response as shown in fig.



a) Ideal



b) Practical

All Pass filter:-

The filter which is used to control the phase response by adding a phase shift between Input and output signals is called as "All Pass filter".

→ The name indicates, it passes all frequencies of Input signal.

→ It does not produce any attenuation but provides the required phase shift for the different frequencies of Input signal.

→ For Example, when signals are transmitted over the transmissio lines, there is change in their phase.

→ To compensate for such phase change, all pass filters are used.

→ Hence, all pass filters are also called as "delay equalizers" (or) "phase correctors"

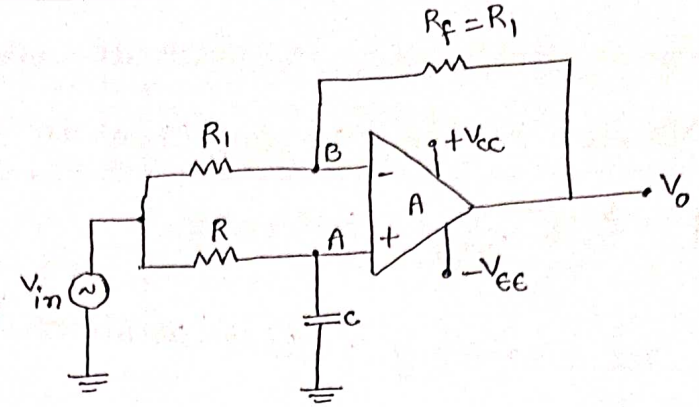


Fig:- First order All pass filter

Analysis :-

Assume, Input to the Non-Inverting terminal zero. The circuit act as an Inverting Amplifier.

$$\therefore V_{o1} = -\frac{R_f}{R_1} V_{in}$$

$$V_{o1} = -V_{in} \quad \text{—①} \quad [\because R_f = R_1]$$

Assume, Input to the Inverting terminal zero. The circuit act as an Non-Inverting Amplifier.

$$V_{o2} = \left(1 + \frac{R_f}{R_1}\right) V_A$$

$$V_{o2} = 2V_A \quad \text{——②} \quad [\because R_f = R_1]$$

By using Potential divider, at V_A.

$$V_A = \left(\frac{-jX_c}{R - jX_c}\right) \cdot V_{in}$$

$$= \left(\frac{\frac{-j}{2\pi fc}}{R - j/2\pi fc}\right) \cdot V_{in} \qquad \left[\because X_c = \frac{1}{2\pi fc}\right]$$

$$= \left[\frac{\frac{1}{j2\pi fc}}{R + \frac{1}{j2\pi fc}}\right] \cdot V_{in} \qquad \left[\because -j = \frac{1}{j}\right]$$

$$V_n = \left[\frac{1}{1+j2\pi fRc}\right] \cdot V_{in} \quad \text{—— (3)}$$

Substitute eq (3) in (2),

$$V_{02} = 2\left[\frac{1}{1+j2\pi fRc}\right] \cdot V_{in} \quad \text{—— (4)}$$

Total output voltage is

$$V_o = V_{o1} + V_{o2}$$

$$= -V_{in} + 2V_{in}\left[\frac{1}{1+j2\pi fRc}\right]$$

$$= V_{in}\left[-1 + \frac{2}{1+j2\pi fRc}\right]$$

$$\Rightarrow \frac{V_o}{V_{in}} = \frac{-1[1+j2\pi fRc]+2}{1+j2\pi fRc}$$

$$= \frac{-1-j2\pi fRc+2}{1+j2\pi fRc}$$

$$\boxed{\frac{V_o}{V_{in}} = \frac{1-j2\pi fRc}{1+j2\pi fRc}} \quad \text{—— (5)}$$

The magnitude of the transfer function is

$$\left|\frac{V_o}{V_{in}}\right| = \frac{\sqrt{1+(2\pi fRc)^2}}{\sqrt{1+(2\pi fRc)^2}} = 1 \quad \text{—— (6)}$$

The magnitude is always 1 for all pass filter and it can pass the entire range of frequency.

Phase angle is given by, $\phi = -\tan^{-1}\left(\frac{2\pi fRc}{1}\right) - \tan^{-1}\left(\frac{2\pi fRc}{1}\right)$

$$\boxed{\phi = -2\tan^{-1}\left(\frac{2\pi fRc}{1}\right)} \quad \text{—— (7)}$$

If $f=0$, $\Rightarrow \phi = 0°$

$f = 1/Rc \Rightarrow \phi = -90°$

$f = \infty \quad \phi = -180°$

This is the phase angle in degrees which indicates that there is a phase shift of ϕ between Input and output signal.

If the positions of R and C are interchanged, we get +ve phase shift.

The -ve phase shift indicates that output V_o lags Input V_{in} by angle ϕ, +ve phase shift indicates that V_o leads Input V_{in} by angle ϕ.

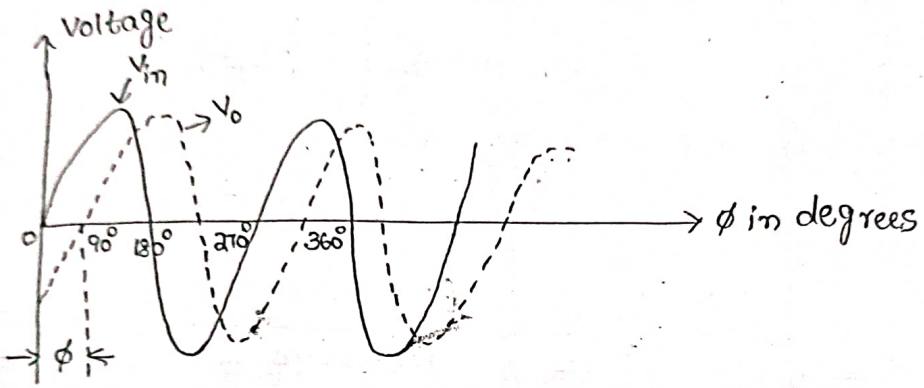


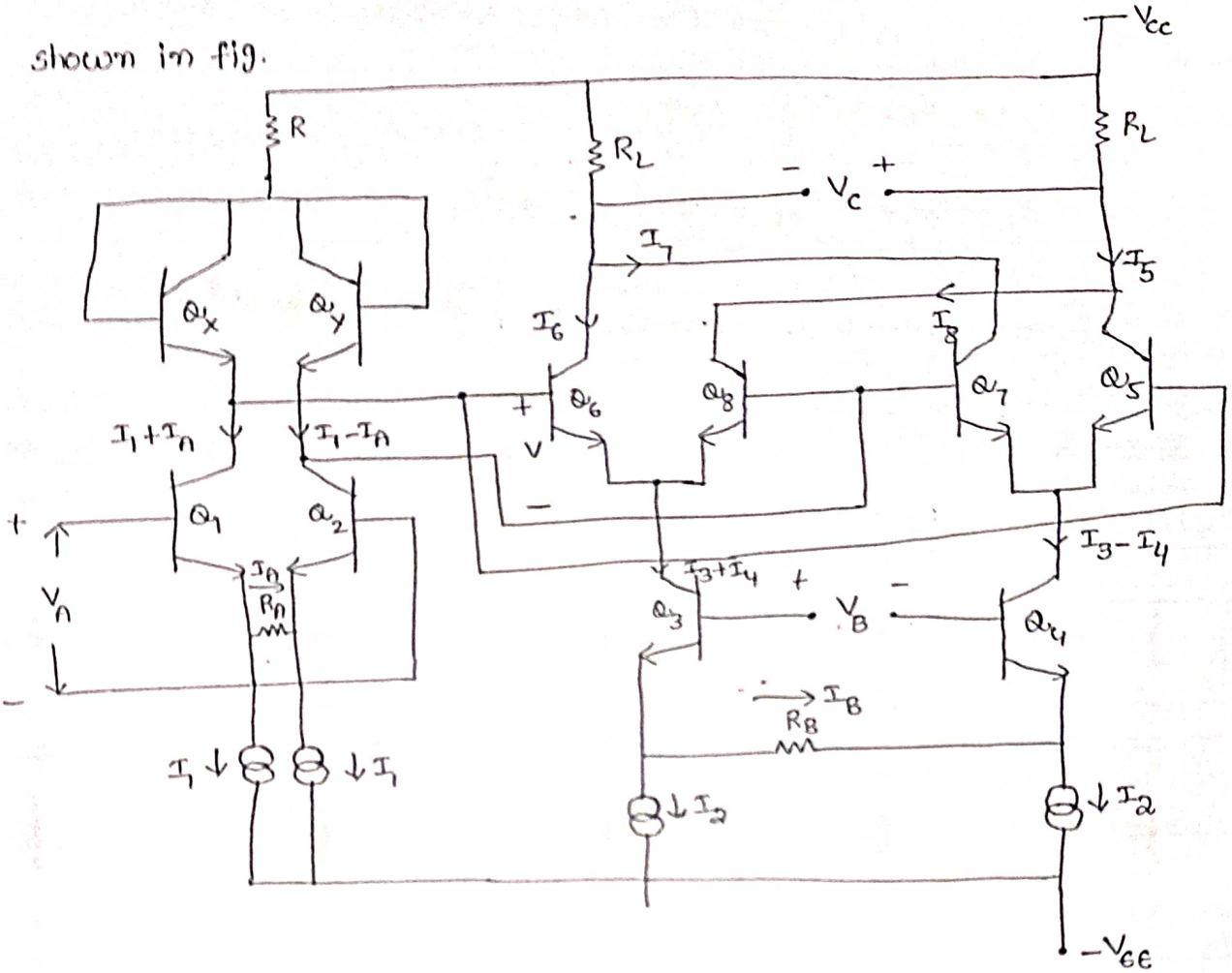
Fig:- Phase shift between V_o and V_{in}.

Four Quadrant multiplier :-

A circuit which can function in all the 4 quadrants of operation and generates the Product of two Input voltages irrespective of the polarity of its Input signals is referred as "Four Quadrant multiplier".

→ It is designed in monolithic form.

The schematic arrangement of 4-Quadrant multiplier as shown in fig.



→ when voltage V_A is applied to the Input of circuit the V_A is Process and result an Intermediate Voltage 'V' generated across Q_x and Q_y.

→ Any Non-linearity signal Involved with in V_A generating V is the Inverse of Non-linearity related with Base emitter Junctions of Q_5-Q_6 and Q_7-Q_8 transistors.

Therefore, output Voltage of circuit is proportional to the linear multiplication of 2 Inputs.

The resistors R_A, R_B called as Emitter degeneration resistors. These resistors is to convert Input voltages into linear differentia currents I_A, I_B.

$$I_A = \frac{V_A}{R_A} \quad , \quad I_B = \frac{V_B}{R_B} \qquad \text{—— (1)}$$

convert voltage to current, R_A and R_B selected as

i) $R_A >> \frac{V_T}{I_1}$

ii) $R_B >> \frac{V_T}{I_2}$

The output voltage is

$$V_{out} = R_L \left[(I_6 + I_7) - (I_5 + I_8) \right] \qquad \text{—— (2)}$$

and

$$\frac{I_6}{I_3 + I_B} = \frac{I_5}{I_3 - I_B} = \frac{I_1 + I_A}{2I_1}$$

$$\Rightarrow I_6 = \frac{(I_3 + I_B)(I_1 + I_A)}{2I_1} \qquad \text{—— (3)}$$

$$\Rightarrow I_5 = \frac{(I_3 - I_B)(I_1 + I_A)}{2I_1} \qquad \text{—— (4)}$$

and also,

$$\frac{I_8}{I_3 + I_B} = \frac{I_7}{I_3 - I_B} = \frac{I_1 - I_A}{2I_1}$$

$$\Rightarrow I_8 = \frac{(I_1 - I_A)(I_3 + I_B)}{2I_1} \qquad \text{—— (5)}$$

$$\Rightarrow R_1 = \frac{(I_3 - I_B)(I_1 - I_A)}{2I_1} \quad \text{---- (6)}$$

substitute equations (2)(4)(5)(6) in eq (3)

$$V_{out} = R_L\left[\left(\frac{(I_3 + I_A)(I_1 + I_A)}{2I_1} + \frac{(I_3 - I_B)(I_1 - I_A)}{2I_1}\right)\right.$$

$$\left. - \left(\frac{(I_3 - I_B)(I_1 + I_A)}{2I_1} + \frac{(I_3 + I_B)(I_1 - I_A)}{2I_1}\right)\right]$$

$$= R_L\left[\left(\frac{I_1 I_3 + I_3 I_A + I_1 I_A + I_A I_A + I_1 I_3 - I_3 I_A - I_1 I_A + I_A I_A}{2I_1}\right)\right.$$

$$\left. - \left(\frac{I_1 I_3 + I_3 I_B - I_1 I_B - I_A I_B + I_1 I_3 - I_3 I_A + I_1 I_B - I_A I_B}{2I_1}\right)\right]$$

$$= R_L\left(\frac{2I_1 I_3 + 2I_A I_B - 2I_1 I_3 + 2I_A I_B}{2I_1}\right)$$

$$= R_L\left(\frac{4 I_A I_B}{2I_1}\right) = 2R_L\left(\frac{I_A I_B}{I_1}\right)$$

as I_A, I_B linearly proportional to V_A, V_B using eq (1), V_{out} can be written as

$$\boxed{V_{out} = K V_A V_B} \quad \left(\because K = \frac{2R_L}{I_1(R_A R_B)}\right)$$

usually, K value is choosen as 0.1

Balanced modulator (IC1496) :-

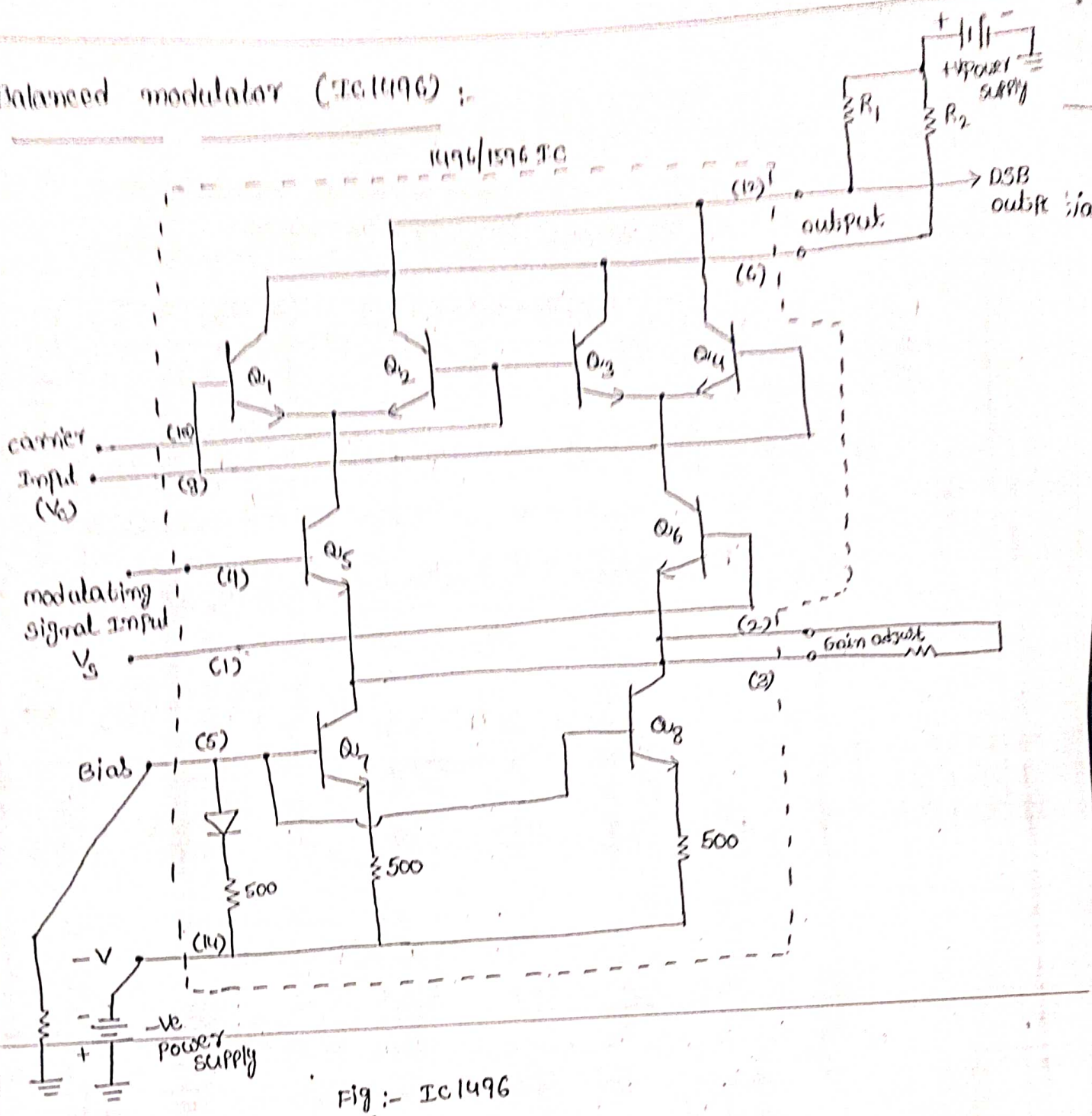


Fig :- Ic1496

→ Transistors Q_7, Q_8 are constant current sources.

→ Transistors Q_1, Q_2, Q_5 form one differential Amplifier and transistors Q_3, Q_4, Q_6 forms another differential Amplifier

→ The constant current sources supply equal amount of current to the two differential Amplifiers.

→ The carrier signal is applied in phase as biasing signal for differential Amplifiers.

→ The modulating signal is applied to the bases of Q_5, Q_6.

→ These transistors are connected in the current paths to the differential transistors, therefore will vary the Amplitude of the current in accordance with the modulating signal.

→ The currents in Q_5, Q_6 will be 180° out of Phase with each other. As current in Q_5 increases, current through Q_6 decreases and vice versa.

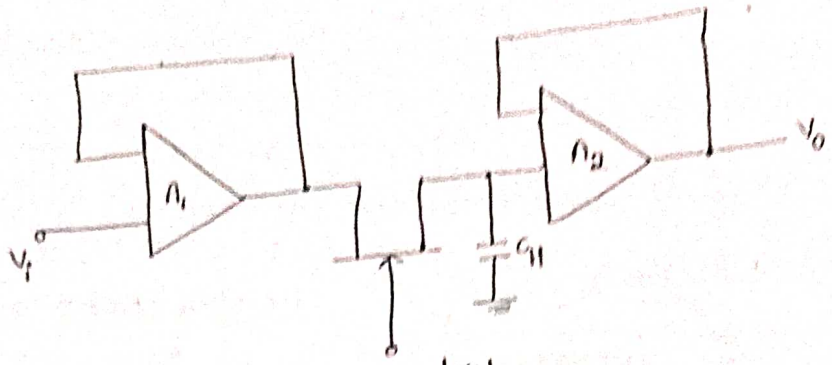
→ From the figure, output of 2- differential Amplifiers connected in Parallel, and output is taken across the two collector terminal of the differential Amplifier.

→ As a result, common signals are get cancelled and only difference signal appears at the output. This suppresses the carrier signal and output we get is the upper and lower side bands.

Sample and Hold circuits :-

In these circuits a JFET is used as switch.

During the sampling time the JFET is turned on, and the holding capacitor charges up to the level of Analog Input voltage.



a) open Loop architecture of sample and Hold circuit

→ Here 2 OP-Amps A_1, A_2 are used. In between these there is E-MOSFET is used as a switch.

→ If E-MOSFET is act as closed switch then the capacitor will charge. If the E-MOSFET is act as open-switch then the capacitor starts discharging.

→ The Acquisition time of S/H circuit is the time required for the holding capacitor C_H to charge upto the level close to the Input voltage during sampling.

→ The acquisition time for S/H circuit is Low as possible.

→ In the circuit, 3 principle factors will control the Acquistion time. These factors are

i) Rc time constant where R is the $r_{ds(ON)}$, i.e on resistance of JFET and 'c' is the holding capacitance C_H.

ii) maximum output current, which can be source (or) sink by

Operational Amplifier

iii) Slew rate of the op-Amp.

→ If the control voltage V_c is at +ve, t-MOSFET is closed switch.
If V_c is at -ve, then t-MOSFET is open switch.

→ Practically, discharging is not possible for this case because,

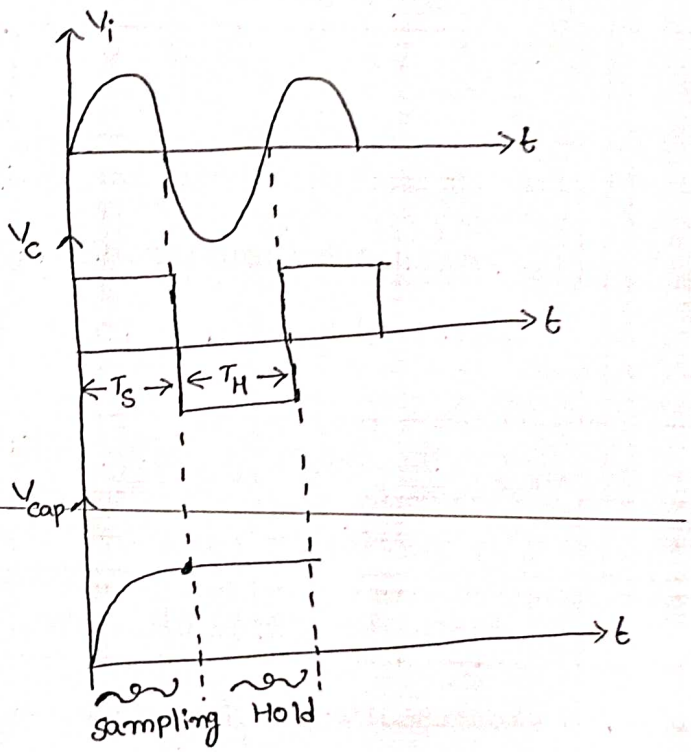
$\tau = RC$

Here $R = \infty$, $\tau = \infty$

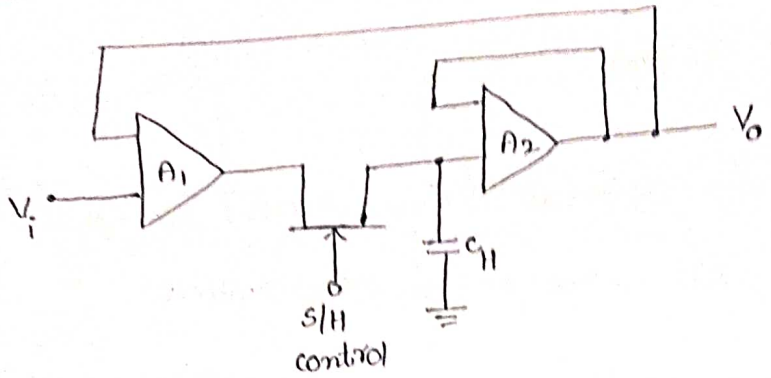
Therefore, discharging time is Infinity.

→ Sampling occurs at the time Interval is $0 < T < T_S$

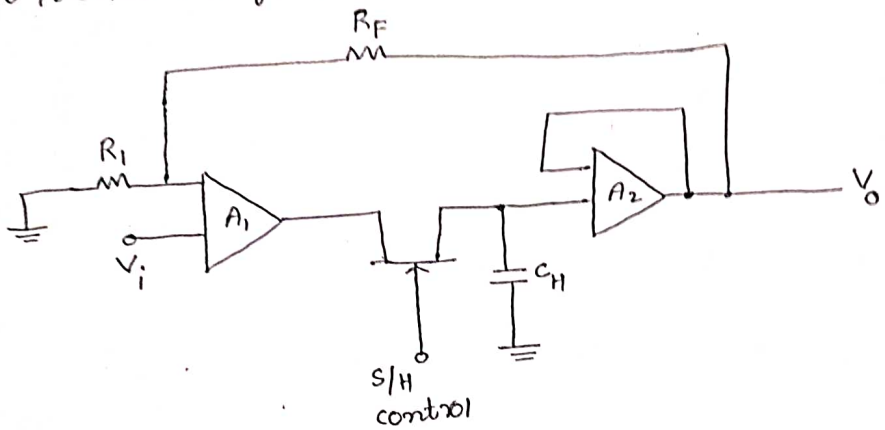
→ Holding occurs at the time Interval is $T_S < T < T_H$.



→ To get maximum output, slew rate of the op-Amp rather than Rc time constant we use the circuit as,



→ To Provide voltage gain, i.e $A = 1 + R_F/R_1$. we use the circuit as

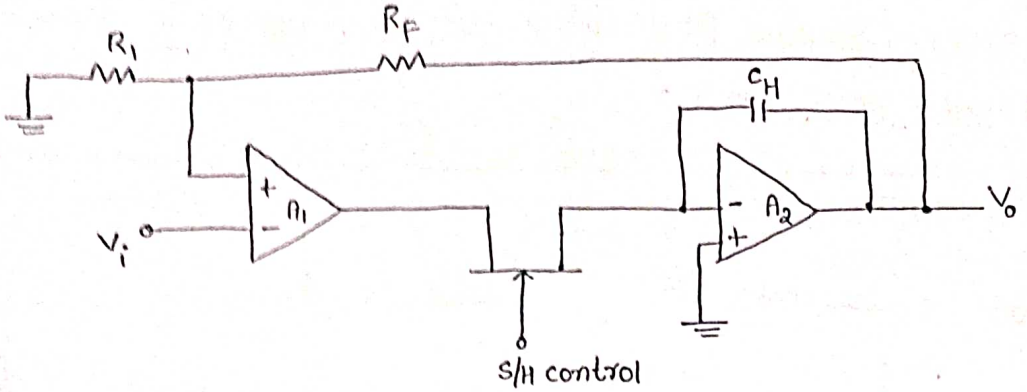


The sampled output voltage is equal to sampled Input voltage multiplied by voltage gain factor of $1 + R_f/R_1$.

→ The following S/H circuit offers 2 advantages

i) The faster capacitor charging rate provides shorter Acquisition tim because, voltage at Inverting Input terminal A_2 equal to capacitor voltage divided by open loop gain of A_2.

ii) In the circuit, summing Input of A_2 remains at Virtual ground. due to this charge removed from summing Junction.



Performance parameters of S/H circuits :- (Extra Syllabus)

1) Acquisition time (t_{ac}):- It is the time required for the holding capaci. C_H to charge up to a level close to Input voltage during sampling.

It depends on

i) Rc time constant

ii) maximum output current

iii) Slew rate of OP-Amp.

2) Aperture time (t_{ap}):-

Because of Propagation delays through driver and switch, V_o will keep tracking V_i some time after the Inception of the hold command. This is the aperture time.

3) Aperture uncertainty (Δt_{ap}) :- It is the variation in aperture time from sample to sample. due to aperture uncertainty it is difficult to compensate aperture time by advancing hold command.

4) Hold mode settling time (t_s):- After the application of hold command, it takes a certain amount of time for V_o to settle with in a specified error band, such as 1%, 0.1% , 0.01% . This is the hold mode

settling time

Problems

1) Design a first order high pass filter at a cut-off frequency of 400 Hz and a passband gain of 1.

Sol:-

Step 1 :- $f_L = 400\ Hz$

Step 2 :- choose 'c' less than 1MF

$C = 0.02 \mu F$

Step 3 :- $f_L = \frac{1}{2\pi RC}$

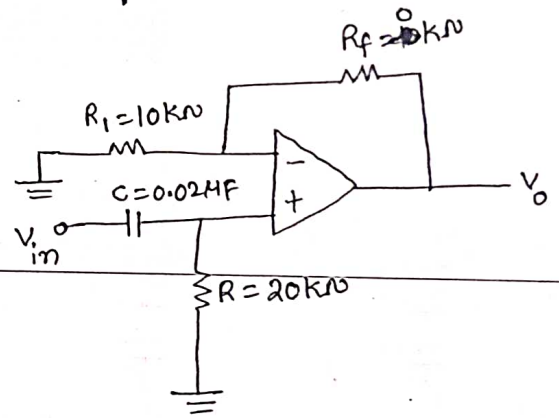
$\Rightarrow R = \frac{1}{2\pi \times 400 \times 0.02 \times 10^{-6}} = 19.8 K\Omega \approx 20 K\Omega$

Step 4 :- $A_F = 1 + \frac{R_f}{R_1} = 1$

$\Rightarrow \frac{R_f}{R_1} = 1 - 1 = 0$

choose $R_f = 0$ i.e unity gain feed back

choose $R_f = 10 K\Omega$



2) Design a first order Lowpass filter so that it has cut-off frequency of 2KHz and a pass band gain of 1.

Sol:-

Step 1 :- $f_H = 2KHz$ Step 2 :- 'c' value choosen as 0.01 MF

Step 3 :- $f_H = \frac{1}{2\pi RC}$

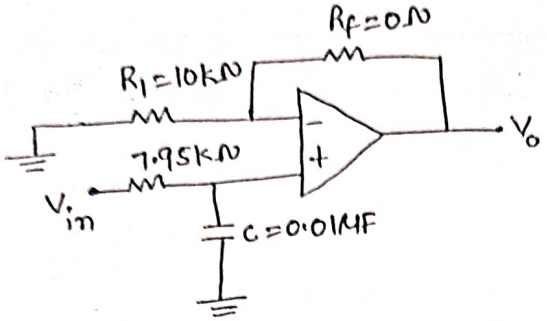
$\Rightarrow R = \frac{1}{2\pi \times f_H \times C} = \frac{1}{2\pi \times 2 \times 10^3 \times 0.01 \times 10^{-6}} = 7.95 K\Omega$

Step 4:- $A_f = 1 + \frac{R_F}{R_1}$

$1 = 1 + \frac{R_F}{R_1} \Rightarrow \frac{R_F}{R_1} = 0$

$\Rightarrow R_f = 0\Omega$

consider $R_1 = 10K\Omega$



3) Design a second order Low Pass Butterworth filter having high cut-off frequency of 1KHz. draw its frequency response.

Step 1:- $f_H = 1KHz$

Step 2:- choose $C_2 = C_3 = C = 0.01\mu F$

Step 3:- choose $R_2 = R_3 = R$

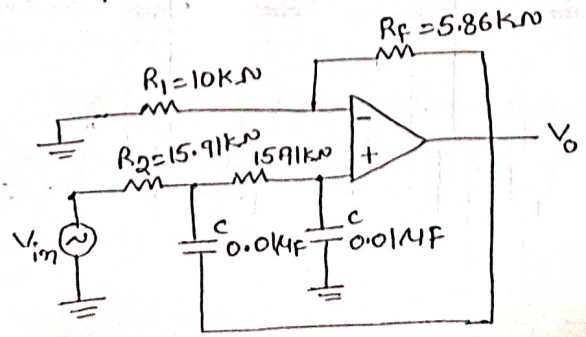
$\Rightarrow f_H = \frac{1}{2\pi RC}$

$\Rightarrow R = \frac{1}{2\pi \times 1 \times 10^3 \times 0.01 \times 10^{-6}} = 15.91K\Omega$

Step 4:- $R_f = 0.586 R_1$ $\quad [\because R_f = 0.586 R_1]$

choose $R_1 = 10K\Omega$

$\Rightarrow R_f = 0.586 \times 10 \times 10^3 = 5.86K\Omega$



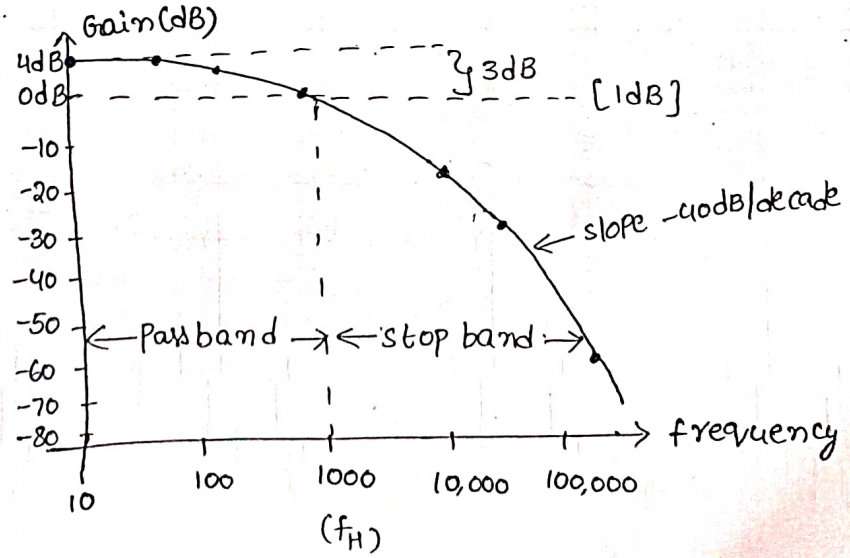
The gain of 2nd order filter is given by

$$\frac{V_o}{V_{in}} = \frac{A_F}{\sqrt{1+(f/f_H)^4}}$$

w.k.t $A_F = 1.586$, $f_H = 1KHz$ $\Rightarrow$ $\frac{V_o}{V_{in}} = \frac{1.586}{\sqrt{1+\left(\frac{f}{1\times10^3}\right)^4}}$

frequency (Hz)	$\frac{V_o}{V_{in}}$	$20\log\left(\frac{V_o}{V_{in}}\right)$
10	1.586	4dB
100	1.585	4dB
500	1.538	3.74dB
1000	1.121	1dB
5000	0.0633	-23.97dB
7000	0.032	-29.89 dB
10,000	0.015	-36.47dB
50,000	6.34×10^{-4}	-63.95 dB
10,0000	1.586×10^{-4}	-76dB

Frequency response



4) Design and obtain the frequency response of a Band pass filter with $f_L = 400Hz$ and $f_H = 1kHz$ with pass band gain 4.

Sol:- Design the low pass filter first:

$f_H = 1kHz$

Let $C = 0.01\mu F$

$$R = \frac{1}{2\pi f_H C} = \frac{1}{2\pi \times 10^3 \times 0.01 \times 10^{-6}} = 15.91\,k\Omega$$

Design the high pass filter,

$f_L = 400Hz$, Let $C = 0.05\mu F$

$$\Rightarrow R = \frac{1}{2\pi f_L C} = \frac{1}{2\pi \times 400 \times 0.05 \times 10^{-6}} = 7.95k\Omega$$

Now $A_{f1} = A_1 A_2 = 1$

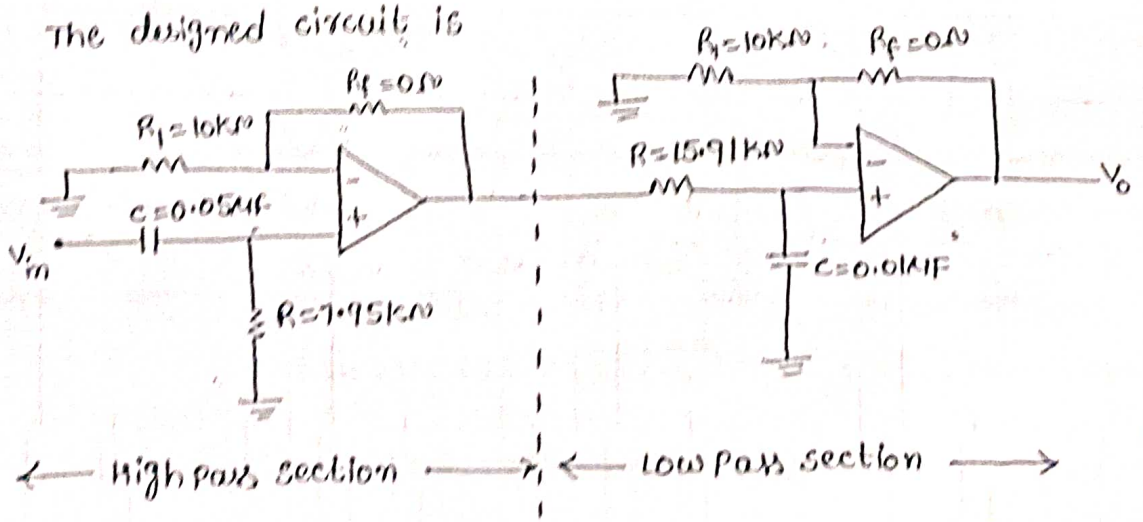
Let $A_1 = A_2 = 1 = 1 + \frac{R_f}{R_1}$

$$\Rightarrow \frac{R_f}{R_1} = 1 - 1 = 0 \Rightarrow R_f = 0\Omega$$

we $R_f = 0\Omega$

& consider $R_1 = 10k\Omega$

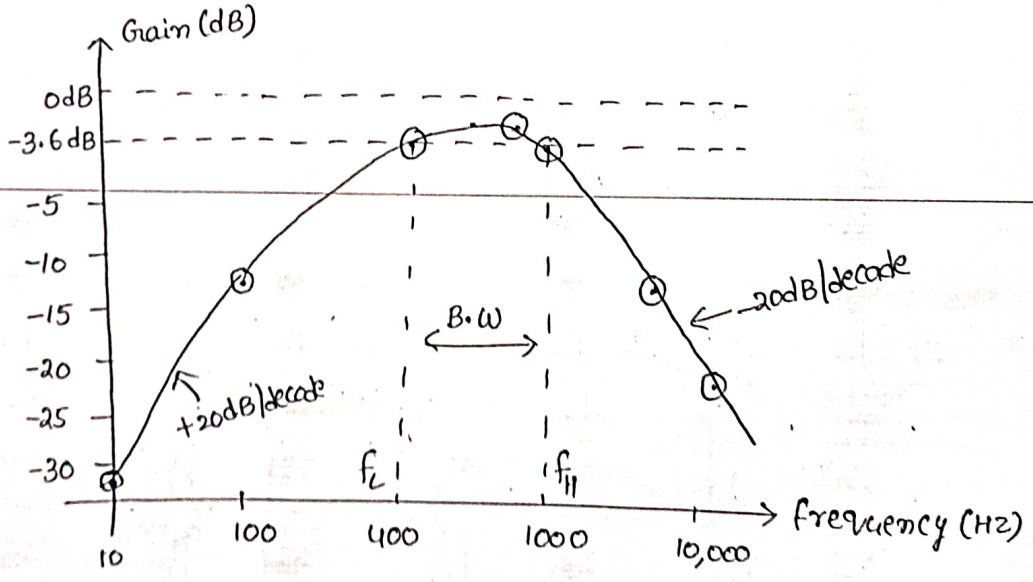
The designed circuit is



Frequency response

$$\left|\frac{V_o}{V_{in}}\right| = \frac{A_{FT}(f/f_L)}{\sqrt{\left[(1+f/f_L)^2\right]\left[(1+f/f_H)^2\right]}} = \frac{f/400}{\sqrt{\left[1+\left(\frac{f}{400}\right)^2\right]\left[1+\left(\frac{f}{1000}\right)^2\right]}}$$

frequency	$\left\|\frac{V_o}{V_{in}}\right\|$	$20\log\left\|\frac{V_o}{V_{in}}\right\|$
10	0.025	-32.04
100	0.241	-12.34
400	0.656	-3.66
600	0.713	-2.93
1000	0.656	-3.66
5000	0.195	-14.17
10,000	0.099	-20.05



Now $f_c = \sqrt{f_L f_H} = \sqrt{400 \times 1000} = 632.45$ Hz

$B.W = f_H - f_L = 1000 - 400 = 600$ Hz

$\therefore Q = \frac{f_c}{B.W} = \frac{632.45}{600} = 1.054$

5) A certain narrow band pass filter has been designed to meet the following specifications: $f_c = 3KHz$, $Q = 25$, $A_F = 10$. what modifications are necessary in the filter circuit to change the center frequency to 1KHz, keeping the gain and bandwidth constant?

Sol:- Choose $C_1 = C_2 = C = 0.02\mu F$

$$R_1 = \frac{Q}{2\pi f_c C A_F} = \frac{25}{2\pi \times 3\times 10^3 \times 0.02 \times 10^{-6} \times 10} = 6.631\,K\Omega$$

$$R_2 = \frac{Q}{2\pi f_c C (2Q^2 - A_F)} = \frac{25}{2\pi \times 3\times 10^3 \times 0.02 \times 10^{-6} (2\times 25^2 - 10)} = 53.48\,\Omega$$

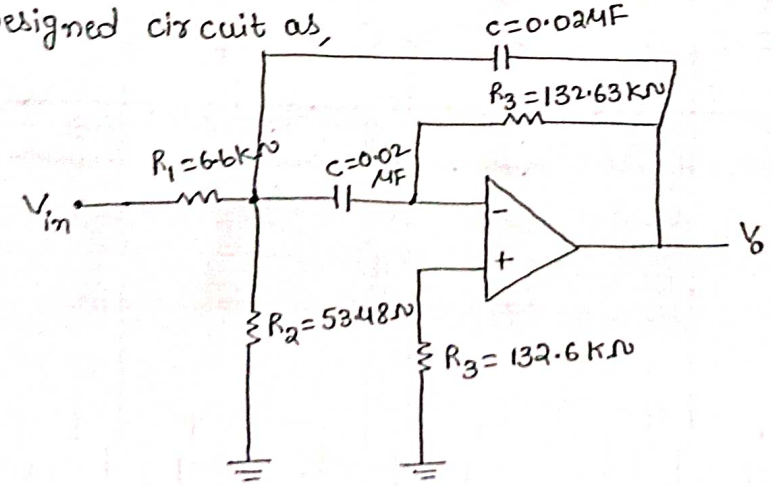
$$R_3 = \frac{Q}{\pi f_c C} = \frac{25}{\pi \times 3\times 10^3 \times 0.02 \times 10^{-6}} = 132.63\,K\Omega$$

change R_2 to R_2', To get f_c' as 1KHz,

$$R_2' = R_2 \left(\frac{f_c}{f_c'}\right)^2$$

$$= 53.48 \times \left(\frac{3\times 10^3}{1\times 10^3}\right)^2 = 481.32\,\Omega$$

Designed circuit as,



6) For all Pass filter, determine the Phase shift between Input and output at f = 2KHz. To obtain positive phase shift what modifications are necessary in the circuit.

Sol:- The phase shift ϕ for all pass filter is,

$$\phi = -2\tan^{-1}[2\pi fRC]$$

G.T $f = 2KHz$, Assume $R = 16K\Omega$, $C = 0.01\mu F$

$$\therefore \phi = -2\tan^{-1}[2\pi \times 2\times10^{3} \times 16\times10^{3} \times 0.01\times10^{-6}]$$

$$= -126.82^{\circ}$$

Thus output lags Input by 126.82° but Amplitude & frequency is same as Input.

* To get +ve Phase shift, Positions of R and C must be Interchanged in All Pass filter.

7) Design all Pass filter with a Phase shift of -135° at a frequency of 2KHz at the output. draw the circuit diagram.

Sol:- G.T $f = 2KHz$, $\phi = -135^{\circ}$

W.K.T $\phi = -2\tan^{-1}[2\pi fRC]$

$$-135 = -2\tan^{-1}[2\pi fRC]$$

$$\Rightarrow 2\pi fRC = \tan(67.5)$$

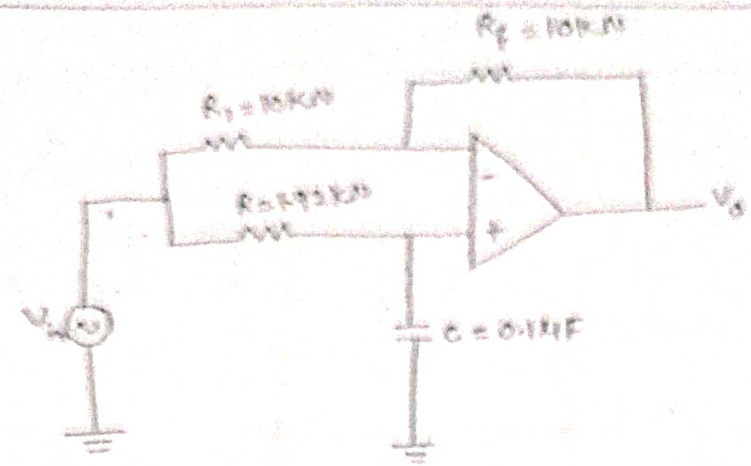
$$\Rightarrow RC = \frac{2.4142}{2\pi \times 2\times10^{3}} = 1.921\times10^{-4}$$

choose $C = 0.1\mu F$

$$\Rightarrow R = 1.92\,K\Omega$$

Let $R_f = R_1 = 10K\Omega$

The designed circuit as,



5) Design an active high pass filter to meet the following specifications.

i) Butterworth response ii) cut-off frequency = 4KHz

iii) Decay rate in the stop band = 40dB/decade.

Sol: G.T, decay rate in stop band is 40dB/decade, it is 2nd order high pass filter.

choose, $C_2 = C_3 = C = 0.02\mu F$

& $f_L = 4Hz$

$$f_L = \frac{1}{2\pi RC} \Rightarrow 4\times10^{3} = \frac{1}{2\pi \times R \times 0.02\times10^{-6}}$$

$$\Rightarrow R = 1.98 \approx 2K\Omega$$

$$R = R_2 = R_3 = 2K\Omega$$

For Butterworth response,

$$A_F = 1.586$$

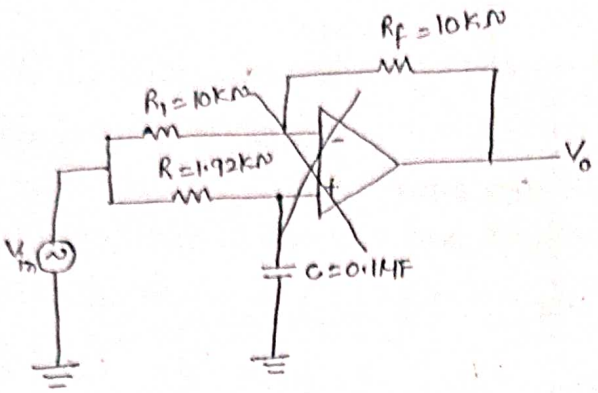
$$= 1 + \frac{R_f}{R_1} \Rightarrow \frac{R_f}{R_1} = 0.586$$

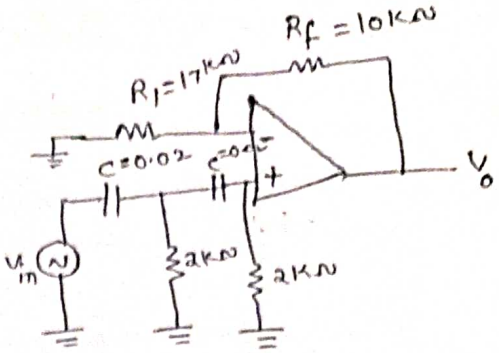
$$\Rightarrow R_f = 0.586 R_1$$

choose $R_f = 10K\Omega$

$$\Rightarrow R_1 = 17K\Omega$$

Hence designed circuit is,





9) Design a notch filter for $f_N = 8KHz$, $Q = 10$. choose $C = 500PF$.

Sol:- use 2nd order Notch filter, $f_N = \frac{1}{2\pi RC}$

$$8\times10^3 = \frac{1}{2\pi \times R \times 500\times10^{-12}}$$

$$\Rightarrow R = 39.7\,K\Omega$$

Now $Q = \frac{1}{2(2-A_f)} \Rightarrow 10 = \frac{1}{2(2-A_f)}$

$$A_f = 1 + \frac{R_f}{R_1} = 1.95$$

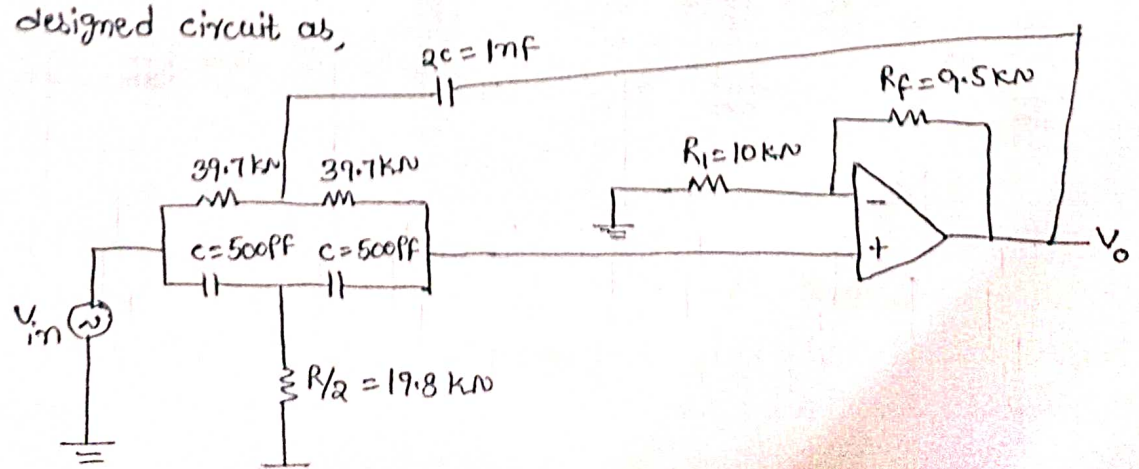
$$\Rightarrow \frac{R_f}{R_1} = 0.95$$

$$\Rightarrow R_f = 0.95 R_1$$

choose $R_1 = 10K\Omega$

$$\Rightarrow R_f = 9.5\,K\Omega$$

designed circuit as,



10) Design a first order wide band-reject filter with a higher cut-off frequency of 100 Hz and lower cut-off frequency of 1KHz. calculate Q- of the filter.

Sol:- G.T $f_H = 100\,Hz$, $f_L = 1KHz$

For high pass section, $f_L = 1KHz$

Assume pass band gain $A_F = 2$.

choose, $C = 0.01\mu F$

$$f_L = \frac{1}{2\pi RC} \Rightarrow R = \frac{1}{2\pi f_L C} = \frac{1}{2\pi \times 10^3 \times 0.01 \times 10^{-6}} = 15.91\,K\Omega$$

For low pass section, $f_H = 100Hz$

Assume pass band gain $A_F = 2$

choose, $C' = 0.05\mu F$

$$f_H = \frac{1}{2\pi R'C'} = \text{---}$$

$$\Rightarrow R' = \frac{1}{2\pi f_H C'} = \frac{1}{2\pi \times 100 \times 0.05 \times 10^{-6}} = 31.83\,K\Omega$$

$$A_F = 1 + \frac{R_f}{R_1} = 2$$

$$\Rightarrow \frac{R_f}{R_1} = 2 - 1 = 1$$

$$\Rightarrow R_f = R_1$$

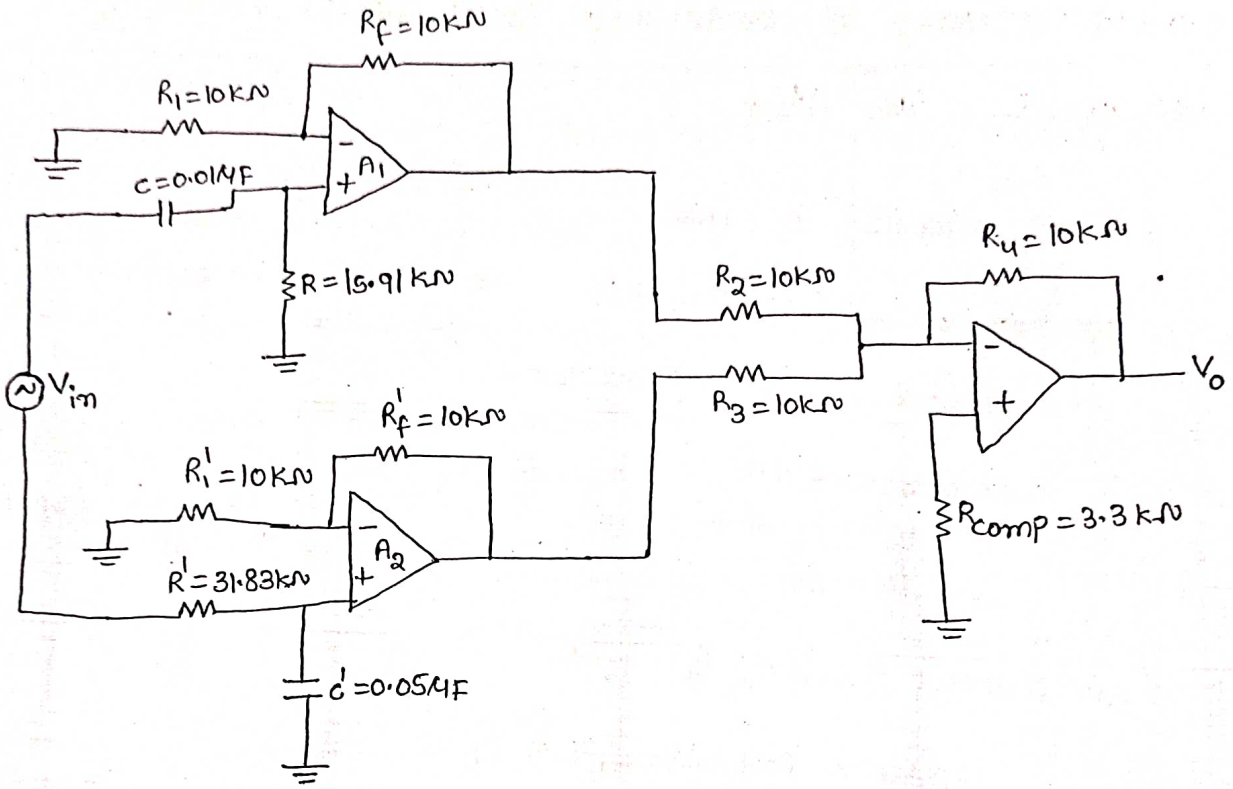
choose $R_f = 10K\Omega \Rightarrow R_f = R_1 = 10K\Omega$

For summing Amplifier, gain be 1.

$$R_2 = R_3 = R_4 = 10K\Omega$$

$$R_{comp} = \frac{R_3}{3} = \frac{10}{3} = 3.33\,K\Omega$$

The designed circuit is,



$$f_c = \sqrt{f_H f_L} = \sqrt{100 \times 1 \times 10^3} = 316.22\,Hz$$

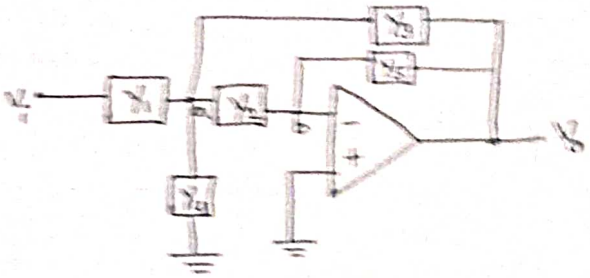
$$B.W = f_L - f_H = 1 \times 10^3 - 100 = 900$$

$$\therefore Q = \frac{f_c}{BW} = \frac{316.22}{900} = 0.3513$$

Narrow band pass filter :-

KCL 'a'

$$Y_1(V_a - V_i) + Y_2(V_a - V_b) + Y_3(V_a - V_o) + Y_4(V_a) = 0$$



Virtual short circuit,

$$V_b = 0$$

$$\Rightarrow Y_1(V_a - V_i) + Y_2(V_a) + Y_3(V_a - V_o) + Y_4 V_a = 0$$

$$\Rightarrow V_a[Y_1 + Y_2 + Y_3 + Y_4] - Y_1 V_i - Y_3 V_o = 0$$

$$\Rightarrow V_a[Y_1 + Y_2 + Y_3 + Y_4] = Y_1 V_i + Y_3 V_o \quad \text{---} \quad (1)$$

KCL 'b'

$$Y_2(V_b - V_a) + Y_5(V_b - V_o) = 0$$

$$\Rightarrow Y_2(0 - V_a) + Y_5(0 - V_o) = 0 \qquad [\because V_b = 0]$$

$$\Rightarrow -V_a Y_2 - Y_5 V_o = 0$$

$$\Rightarrow -V_a Y_2 = Y_5 V_o$$

$$\Rightarrow V_a = \frac{-Y_5 V_o}{Y_2} \quad \text{---} \quad (2)$$

Sub eq (2) in (1)

$$\Rightarrow \frac{-Y_5 V_o}{Y_2}[Y_1 + Y_2 + Y_3 + Y_4] = Y_1 V_i + Y_3 V_o$$

$$\Rightarrow -Y_5 V_o [Y_1 + Y_2 + Y_3 + Y_4] = Y_2[Y_1 V_i + Y_3 V_o]$$

$$\Rightarrow -V_o[Y_5[Y_1 + Y_2 + Y_3 + Y_4]] = Y_2 Y_1 V_i + Y_2 Y_3 V_o$$

$$\Rightarrow -V_o[Y_5(Y_1 + Y_2 + Y_3 + Y_4)] - Y_2 Y_3 V_o = Y_1 Y_2 V_i$$

$$\Rightarrow -V_o[Y_5(Y_1 + Y_2 + Y_3 + Y_4) + Y_2 Y_3] = Y_1 Y_2 V_i$$

$$\Rightarrow \boxed{\frac{V_o}{V_i} = \frac{-Y_1 Y_2}{Y_5[Y_1+Y_2+Y_3+Y_4]+Y_2 Y_3}}$$

For KCL,

$Y_1 = G_1 = \frac{1}{R_1}$

$Y_2 = sC_2$

$Y_3 = sC_3$

$Y_4 = G_4 = \frac{1}{R_4}$

$Y_5 = G_5 = \frac{1}{R_5}$

$$\Rightarrow \frac{V_o(s)}{V_i(s)} = \frac{-sC_2 G_1}{G_5(G_1+sC_2+sC_3+G_4)+s^2 C_2 C_3}$$

$$\Rightarrow H(s) = \frac{-sC_2 G_1}{s^2 C_2 C_3 + sG_5(C_2+C_3)+G_5(G_1+G_4)}$$

$$\Rightarrow H(s) = \frac{-sC_2 G_1}{s^2 + s\frac{G_5(C_2+C_3)}{C_2 C_3} + \frac{G_5(G_1+G_4)}{C_2 C_3}}$$

compare above equation with $\frac{1}{s^2+2\xi\omega_n s+\omega_n^2}$

$$\Rightarrow \omega_n^2 = \frac{G_5(G_1+G_4)}{C_2 C_3}$$

$$\Rightarrow \boxed{\omega_0 = \sqrt{\frac{G_5(G_1+G_4)}{C_2 C_3}}}$$

* Resonant frequency, $\left.\frac{V_o}{V_i}\right|_{\omega=\omega_0} = \frac{-G_1 C_2}{G_5(C_2+C_3)}$

* Quality factor, $Q_0 = \frac{\omega_0 C_2 C_3}{G_5(C_2+C_3)}$

* Band width $= \frac{G_5(C_2+C_3)}{2\pi \cdot C_2 C_3}$

* Choose $C_2 = C_3 = C$

i) $\omega_0 = \sqrt{\dfrac{G_{15}(G_1 + G_{14})}{C}}$

ii) $\left.\dfrac{V_0}{V_1}\right|_{\omega=\omega_0} = \dfrac{-G_1 C}{G_{15}(C+C)} = \dfrac{-G_1 2}{2 G_{15}} = \dfrac{-G_1}{2G_{15}}$

$= \dfrac{-R_5}{2R_1} = -A_0$

$$\boxed{A_0 = \frac{R_5}{2R_1}}$$

iii) $Q_0 = \dfrac{\omega_0 \cdot C \cdot C}{G_{15}(C+C)} = \dfrac{\omega_0 C^2}{2 C G_{15}}$

$= \dfrac{\omega_0 C}{2 G_{15}} = \dfrac{\omega_0 C R_5}{2}$

iv) Bandwidth $= \dfrac{G_{15}(C+C)}{2\pi \cdot CC} = \dfrac{G_{15}(2C)}{2C^2\pi} = \dfrac{G_{15}}{\pi C} = \dfrac{1}{R_5 \cdot \pi C}$

Problems

1) choose $C < 1\mu F$

2) $R_5 = \dfrac{2Q_0}{\omega_0 \cdot C} = \dfrac{2Q_0}{2\pi f_0 C} = \dfrac{Q_0}{\pi f_0 C}$

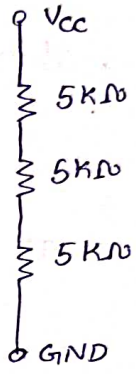
3) $R_1 = \dfrac{R_5}{2A_0} = \dfrac{Q_0}{\pi f_0 C \cdot 2A_0} = \dfrac{Q_0}{\pi f_0 C \cdot 2A_0}$

4) $R_4 = \dfrac{Q_0}{2\pi f_0 C (2Q_0^2 - A_0)}$ [$\because$ choose $2Q_0^2 > A_0$ otherwise we get -ve value].

G. Venkata Hanuman
Asst. Prof

5. Timers and Phase Locked Loop

Timers:- IC 555 is Linear IC which is mostly used to caluclate accurately time delays. Internally it has series combination of three 5KΩ resistors so it called as "555-timer".



* Packages of 555 timer are
  1. 8-pin min. DIP
  2. 14-pin DIP
* By using Single 555 timer, we can generate time delays of range 4sec to hours.
* In XR-2240 timer, we have one 555 timer and one Programmable binary counter.
* In 556 timer it has consists of two 555 timers.

Features:-

* It has range of 4sec to hours
* It has wide range of supply voltages, $V_{cc} = +5V$ to $+18V$ so that it is verstatile and easy to use, reliable and less cast.
* It can Produce a load current of 200mA (or) It can deliver a output load current of 200mA.
* By using 555 timer, it is possible to adjust the duty cycle i.e by using 555 timers we can generate square wave and triangular waves.

* It can operate in wide range of temperatures

* It is designed for operating temperatures ranging from

$-55^{\circ}C$ to $+125^{\circ}C$ for NE 555 timer

$0^{\circ}C$ to $70^{\circ}C$ for SE 555 timer

* It has a temperature stability of 50 PPm/°C change is temperature

50 PPm/°C $\approx$ 0.005%/°C

* It is compatible with Both TTL and cmos logic families

i) In TTL, → Power dissipation is high

→ speed of operation is high

ii) In cmos, → Less Power dissipation

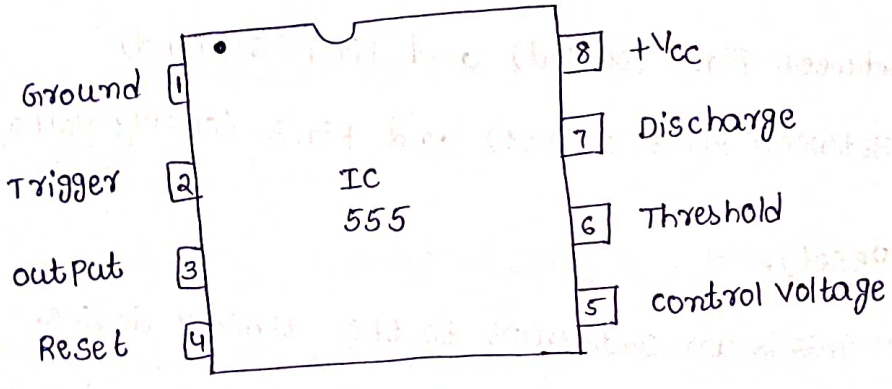
→ speed of operation is low

Applications of IC 555 timer :-

1. mono stable multivibrator
2. Astable multivibrator
3. DC-DC converters
4. Digital Logic Probes
5. oscillators
6. waveforms generators such as Ramp, Pulse, square wave forms.

7. Analog frequency meters & Tachometers
8. Temperature measurements and control
9. Infrared (IR) transmitters
10. Buggler Alarm's and toxic gas alarms
11. Voltage regulator and voltage monitors
12. Traffic light control

Pin diagram of IC 555 timer :- (IC NE 555 timer)



Functions of Pins :- (Pin descriptions)

Pin 1 : Ground :-

All the voltages are measured with respect to this terminal

Pin 2 :- Trigger :-

The IC 555 uses 2 comparators. The voltage divider consists of three equal resistances. Due to voltage divider, the voltage of Non Inverting terminal of comparator 1 & is fixed at $V_{cc}/3$ V_{cc} The Non Inverting Input of comparator 2. which is

compared with $V_{cc}/3$.

The output of timer changes from one state to another i.e if the voltage at this pin becomes greater than $\frac{2}{3}V_{cc}$ then output will be Low.

If the voltage at this pin becomes lower than $\frac{1}{3}V_{cc}$ then output will be High.

Pin 3 (Output):- It is the output pin. A load is connected to this pin.

→ Load can be connected in 2 ways

i) Between Pin 3 (output) and Pin 1 (Ground)

ii) Between Pin 3 (Output) and Pin 8 (supply voltage).

Pin 4 (Reset):-

This is an Interrupt to the timing device. When Pin 4 is grounded, it stops the working of device and makes it off. Thus, Pin 4 provides on/off feature to the IC 555. Input overrides all other functions with in the timer when it is momentarily grounded.

Pin 5 (control voltage Input):-

In most of the applications, external control voltage Input is not used. This pin is nothing but Inverting input terminal of comparator 1. The voltage divider holds the voltage of this input at $\frac{2}{3}V_{cc}$. This is reference level of comparator 1 with

which threshold is compared. If reference level required is other than $\frac{2}{3}V_{cc}$ for comparator 1 then External Input is to be given to Pin 5.

Pin 6 (Threshold):-

This pin is connected to Non-Inverting Input terminal of comparator 1. The external voltage is applied to Pin 6. when this voltage is more than $\frac{2}{3}V_{cc}$, comparator 1 output goes high. due to this output of timer becomes Low.

Remember that output at Pin 3 is $\bar{Q}$ which is complementary output of flipflop.

For threshold $> \frac{2}{3}V_{cc}$, flipflop → set, Q → High, output at Pin 3 → Low

For trigger $< \frac{1}{3}V_{cc}$, flip flop → Reset, Q → Low, output at Pin 3 → High

Pin 7 (Discharge):-

This pin is connected to collector of discharge transistor Q_1. If the output of timer is Low, Q_1 is ON which in turn connects the external capacitor to ground. If the output timer is High, Q_1 OFF which in turn disconnects the external capacitor from ground.

Pin 8 (supply voltage $+V_{cc}$):-

The IC 555 timer can work with any supply voltage between 4.5V and 16V.

Functional diagram of 555 timer (or) significance of Each comparator in 555 timer

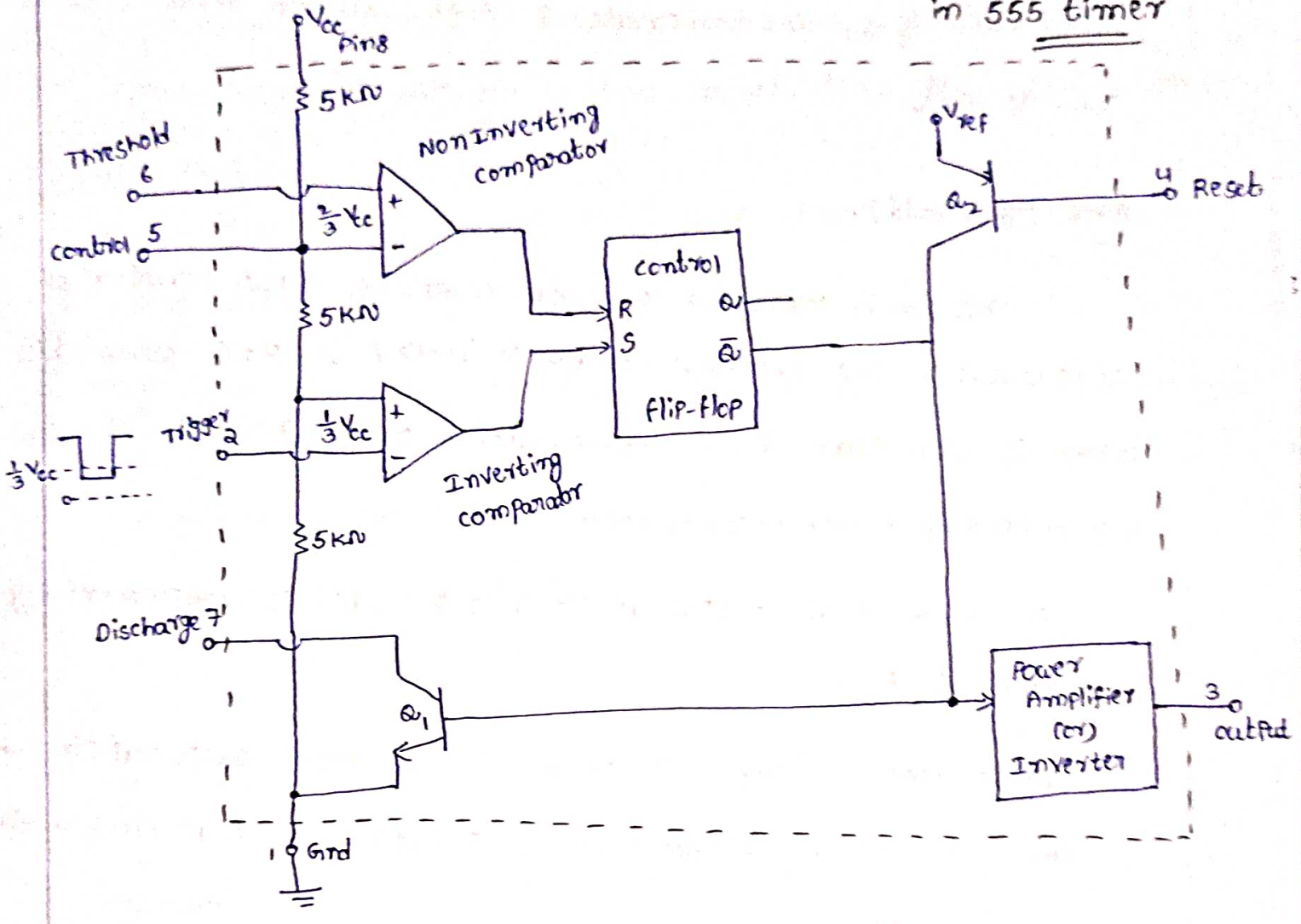


Fig:- Functional diagram of 555 Ic timer

Ic 555 timer contains,

i) 2-comparators, Non Inverting comparator (upper comparator) and Inverting comparator (lower comparator)

ii) A potential divider network formed by three 5KΩ resistors

iii) A Power amplifier (or) Inverter

iv) control flip-flop

v) Buffer transistor & discharging transistor

→ The voltage divider provides a voltage of $\frac{2}{3}V_{cc}$ to the Inverting Input of upper comparator and $\frac{1}{3}V_{cc}$ to the Non Inverting Input of Lower comparator. These 2 voltages forms threshold voltage levels of upper and Lower comparators. Therefore, they helps to find timing Interval. Hence, the time can be varied by applying modulation voltage to control Pin.

→ Initially, Assume that timer is in Stable state (or) stand by mode. in this state, output $\bar{Q}$ of control flip flop is High and it is applied to Power Amplifier.

Power Amplifier is Nothing but an Inverter, i.e High level signal applied to its input to Low level signal. hence output of timer becomes Low.

→ A Negative going external trigger is applied to trigger Pin (i.e Inverting input of Lower comparator). Here D.c level of -ve trigger pulse should be greater than Lower threshold voltage i.e $\frac{V_{cc}}{3}$.

when ever -ve trigger passes through Lower threshold voltage, the lower comparator provides High output.

Due to this the output of $\bar{Q}$ of control flip flop changes to Low & Q to High (i.e $Q=1$, $\bar{Q}=0$). Therefore, output of timer at Pin 3 becomes High.

→ when threshold voltage at Non-Inverting Input of upper comparator exceeds $\frac{2}{3}V_{cc}$, the output of upper comparator becomes High.

Due to this output $\bar{Q}$ of control flip flop changes back to High ($Q=0, \bar{Q}=1$)

Therefore, the output of timer at pin3 becomes Low. Thus IC 555 timer works.

→ The Pin4 (Reset Pin) is used to reset the timer so as to override the operation of lower comparator.

When the reset is not used it is connected to V_{cc}. The transistor Q_2 energized by internally available reference voltage V_{ref}, act as buffer and it is used to Isolate the reset input from control flip-flop and discharge transistor Q_1.

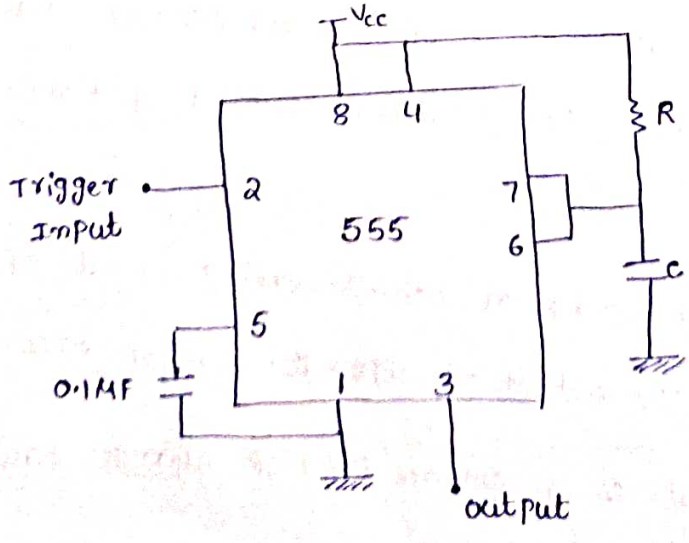
→ when $\bar{Q}$ of flip flop is Low, the discharge transistor Q_1 will be in OFF condition & Pin7 is open.

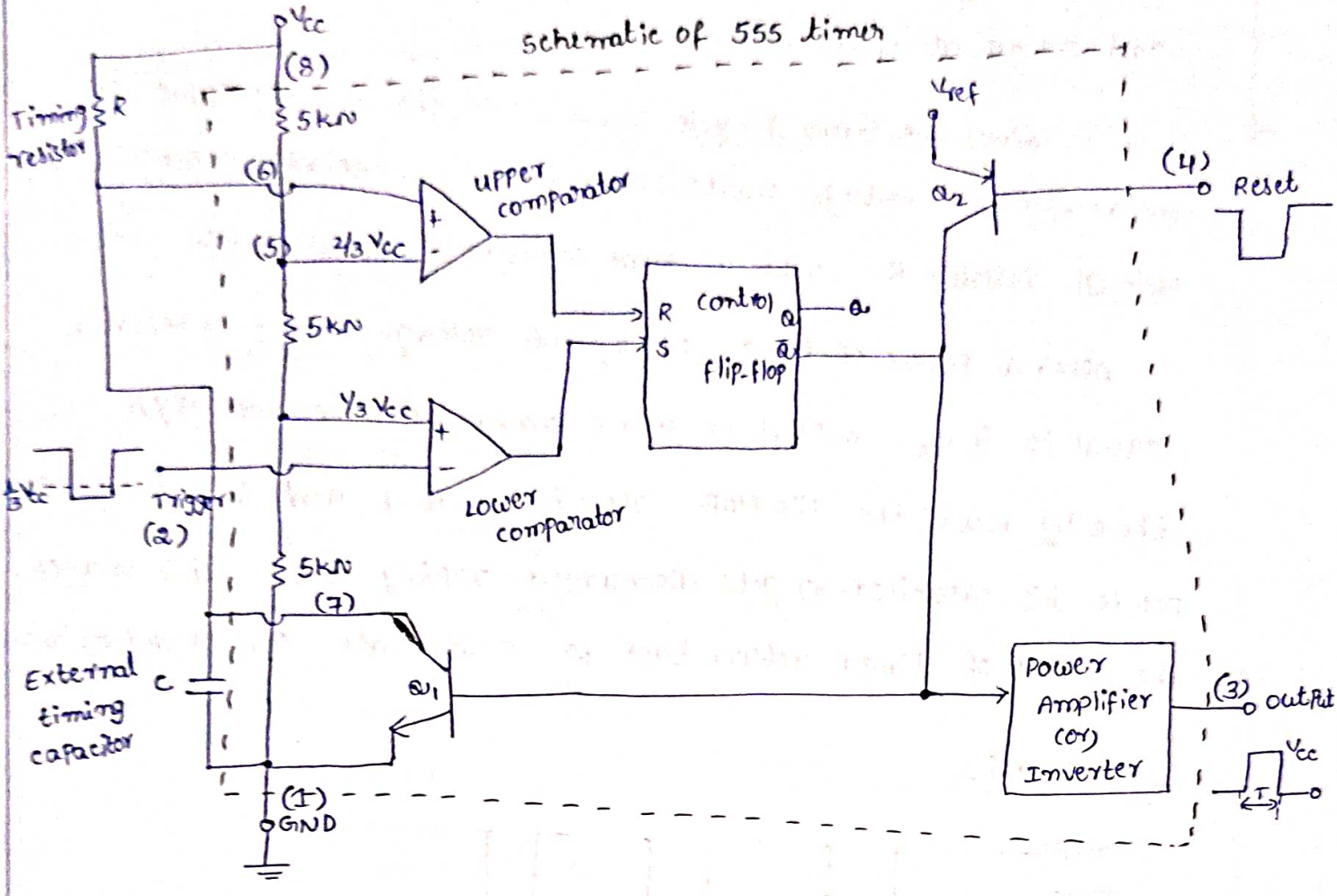
→ when $\bar{Q}$ of flipflop is High, Q_1 becomes forward biased and conducts due to which Pin7 will be connected to ground.

monostable multivibrator:-

The circuit has one stable state and one Quasi stable state. It also called as one-shot (or) mono shot multivibrator.

The functional schematic arrangement as,





Initially, Assume that the timer is in stable state (or) stand by mode.

In this state output $\bar{Q}$ of control flip flop is High & it is given to transistor Q_1. Therefore, Q_1 is ON, due to which the external timing capacitor gets clamped to ground (i.e short circuit to ground). Thus the output of timer will be ground potential i.e Low.

Now, when an externally applied -ve going trigger pulse passes through Lower threshold voltage ($\frac{1}{3}V_{cc}$), the output of Lower comparator is High. Therefore, output $\bar{Q}$ of flipflop changes to Low i.e $\bar{Q}=0$. due to this transistor Q_1 will be turned OFF.

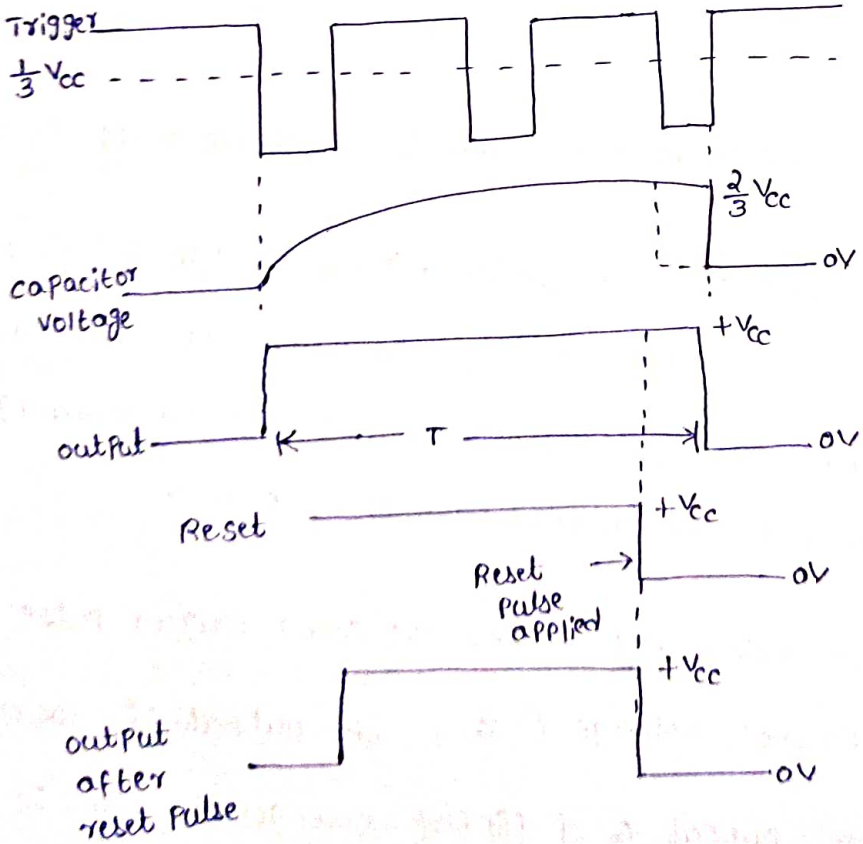
Therefore, timing capacitor gets unclamped (disconnected from ground)

and output at times becomes High.

Now, the timing cycle starts. As the timing capacitor is unclamped its voltage starts Increase exponentially towards V_{cc} through resistor R with a time constant equal to RC.

After a Period of time, say T, the voltage across c becomes equal to $\frac{2}{3}V_{cc}$, output of upper comparator becomes High there by resets the flip flop. Therefore, $\bar{Q}=1$ and Q_1 becomes ON. Due to this capacitor c gets discharged rapidly to 0V. This makes the output of timer return back to stable state (or) stand by mode.

Waveforms :-



Derivation of pulse width :-

Voltage across capacitor Increases exponentially and is given by

$$V_c = V_{cc}(1-e^{-t/RC})$$

If $V_c = \frac{2}{3}V_{cc}$

$$\Rightarrow \frac{2}{3}V_{cc} = V_{cc}(1-e^{-t/RC})$$

$$\Rightarrow \frac{2}{3} = 1-e^{-t/RC}$$

$$\Rightarrow \frac{2}{3}-1 = -e^{-t/RC} \qquad \Rightarrow \frac{1}{3} = e^{-t/RC}$$

$$\Rightarrow -t/RC = \ln\left(\frac{1}{3}\right)$$

At $t=T$

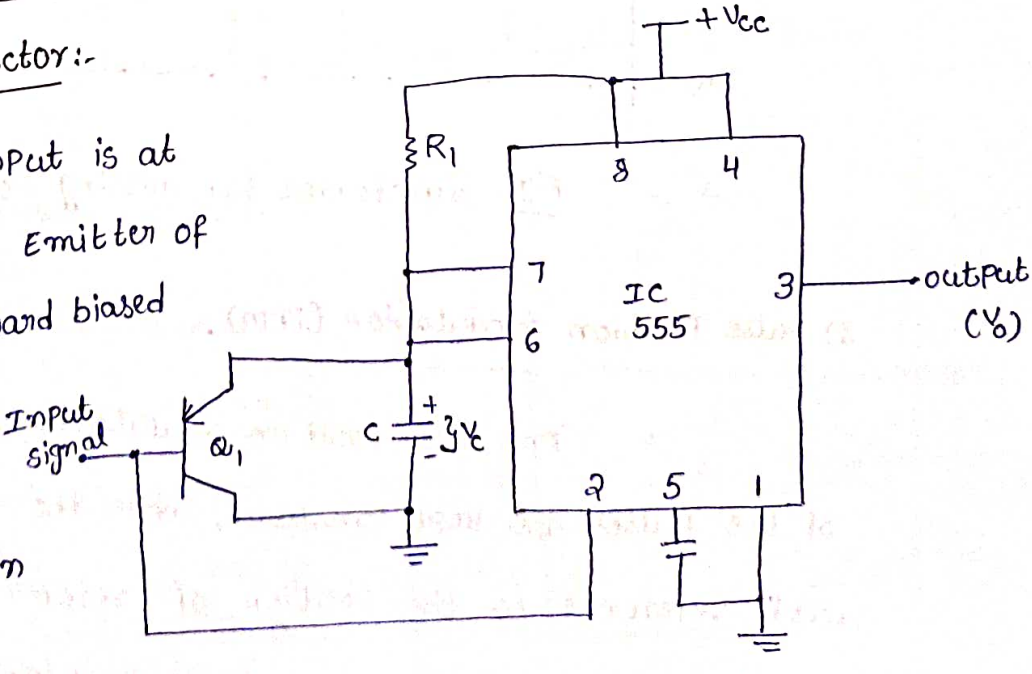
$$\Rightarrow \frac{-T}{RC} = \ln\left(\frac{1}{3}\right)$$

$$\Rightarrow \boxed{T = 1.1RC}$$

Applications of monostable multivibrator :-

1. missing pulse detector :-

when signal Input is at ground level (0V), Emitter of transistor Q_1 forward biased and clamps capacitor voltage V_c to 0.7V i.e output in high state.



when signal Input goes high, the transistor cut-off and capacitor begins to charge.

If Input signal again goes low before the 555 completes its timing cycle, voltage across 'c' resets to 0.7V.

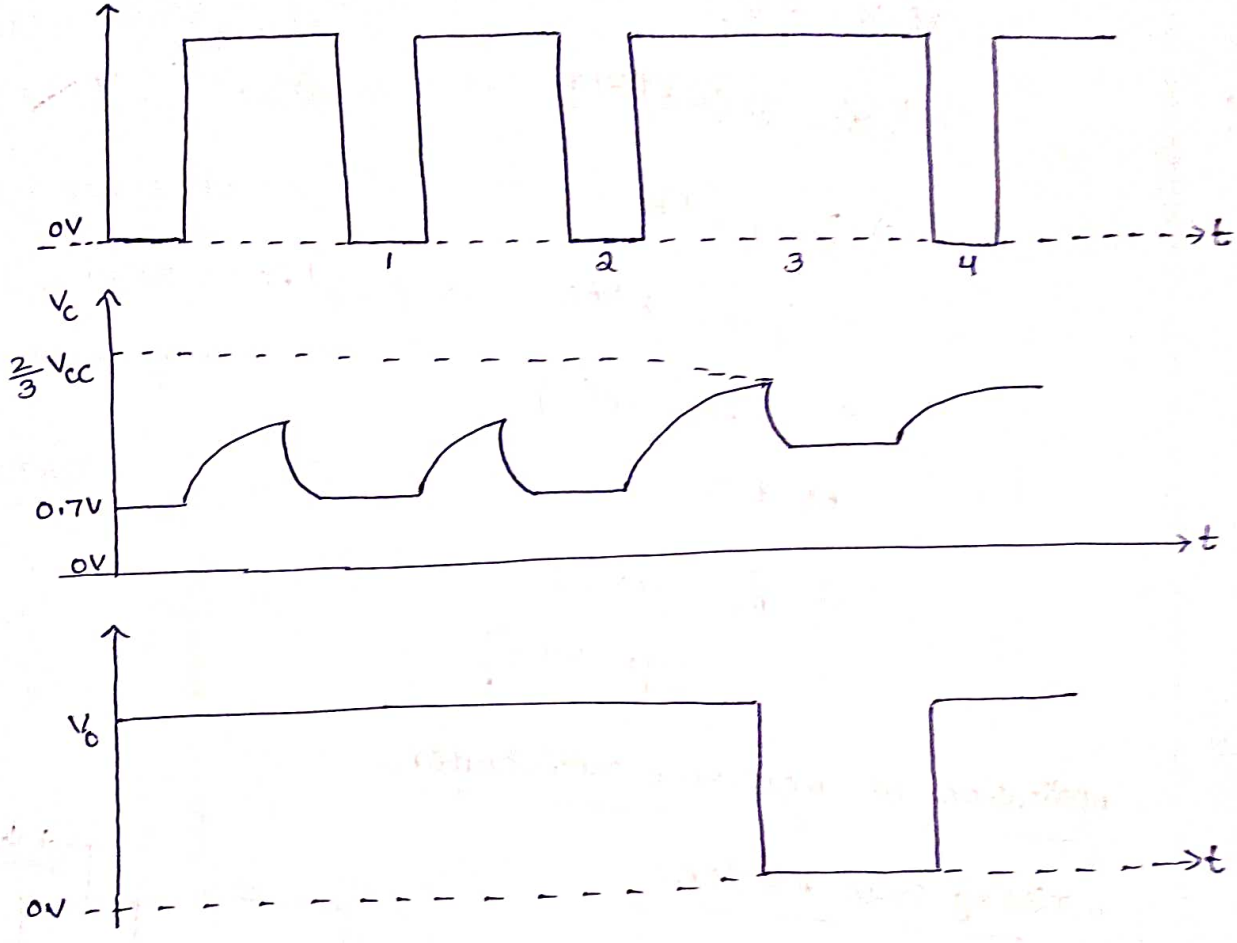


Fig:- waveforms for missing Pulse detector

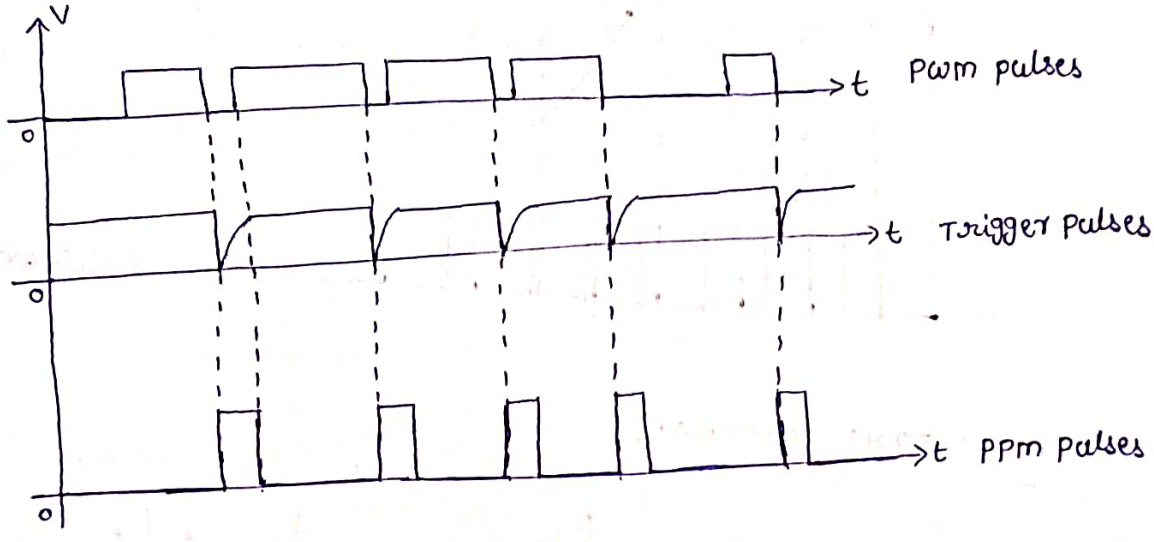
2) Pulse Position modulation (PPm) :-

In Pulse Position modulation, the amplitude & width of the Pulses are kept constant, while the Position of each Pulse with reference to the Position of reference Pulse, is changed according to Instantaneous sampled value of modulating signal.

It consists of differentiator and a monostable multivibrator. The Input to the differentiator is a PWM waveform. The differentiator generates +ve and -ve spikes corresponding to leading and trailing edges of the PWM waveform.

Diode D_1 is used to bypass the +ve spikes. The -ve spikes are used to trigger monostable multivibrator.

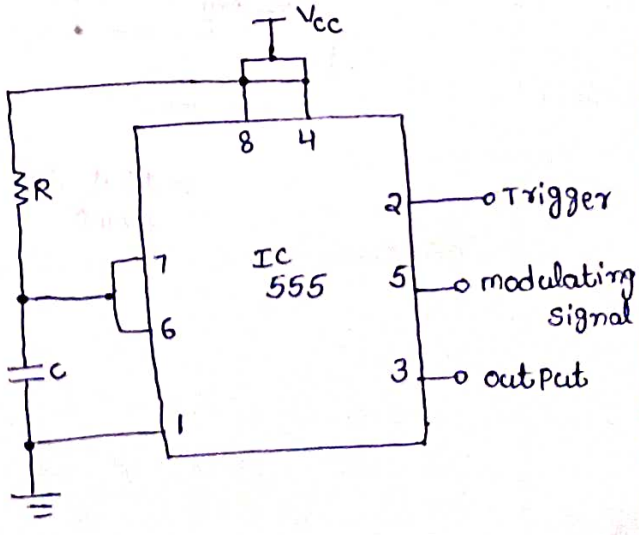
The monostable multivibrator generates the pulses of same width and Amplitude with reference to trigger to give Pulse Position modulated waveform.



3) Pulse width modulation (PWM) :-

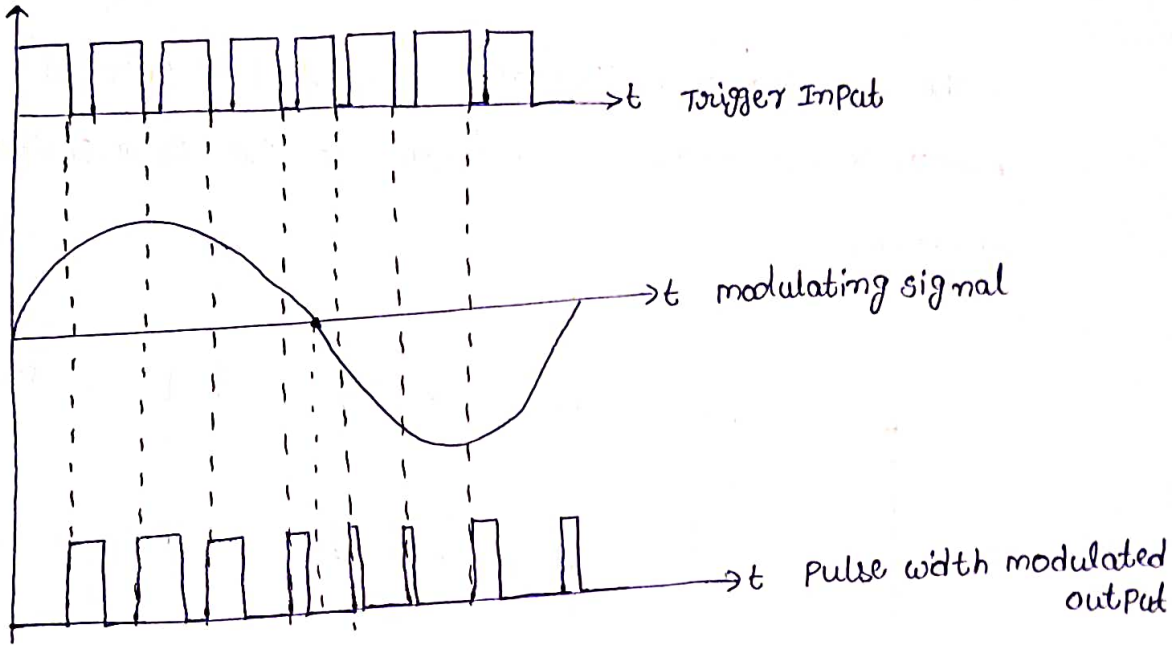
It is basically Pals monostable multivibrator with a modulating Input signal applied at control voltage Input (Pin5).

Internally, control voltage is

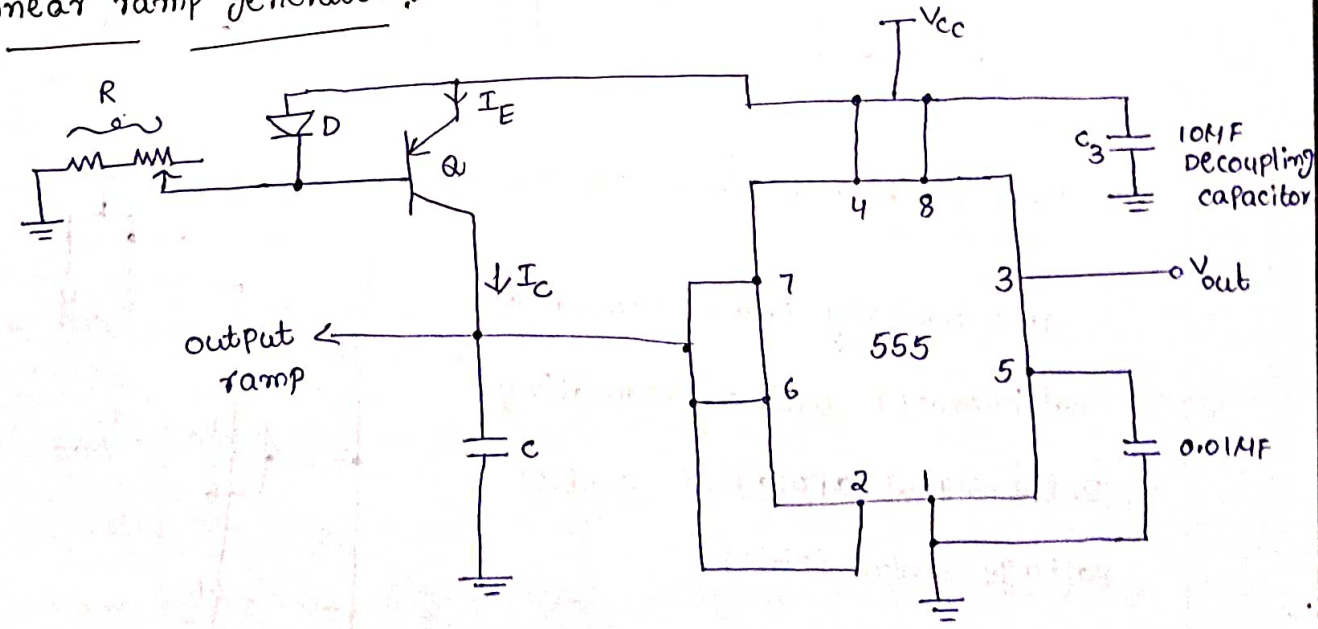


is adjusted to 2/3 V_{cc}.

→ Externally applied modulating signal changes the control voltage, and hence threshold voltage level of upper comparator. As a result, time period required to charge the capacitor upto threshold voltage level changes, giving pulse width modulated signal at the output.



H) Linear ramp generator :-



when a capacitor is charged with a constant current source then linear ramp is obtained.

→ The circuit is used to obtain constant current I_C is a current mirror circuit, using transistor Q and diode D.

→ The current I_C, charges capacitor C at a constant rate towards $+V_{cc}$.

→ Voltage at Pin 6 i.e capacitor voltage V_C becomes $\frac{2}{3}V_{cc}$, the comparator makes internal transistor Q_1 ON with in no time.

But while discharging when V_C becomes $\frac{1}{3}V_{cc}$, the 2nd comparator makes Q_1 OFF & 'C' starts charging again.

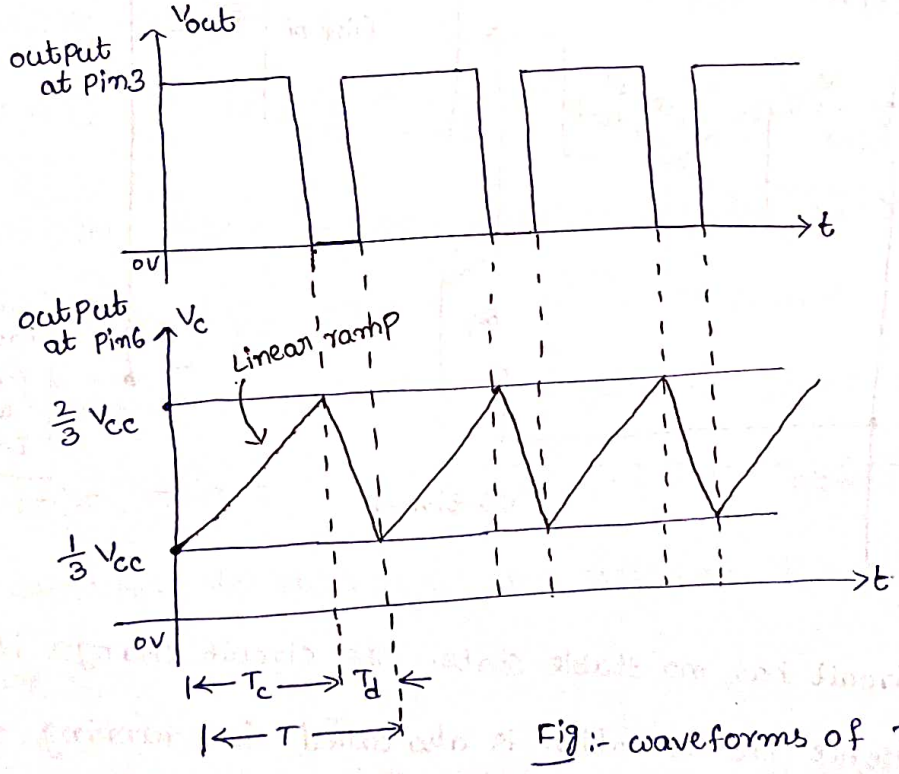


Fig :- waveforms of ramp generator

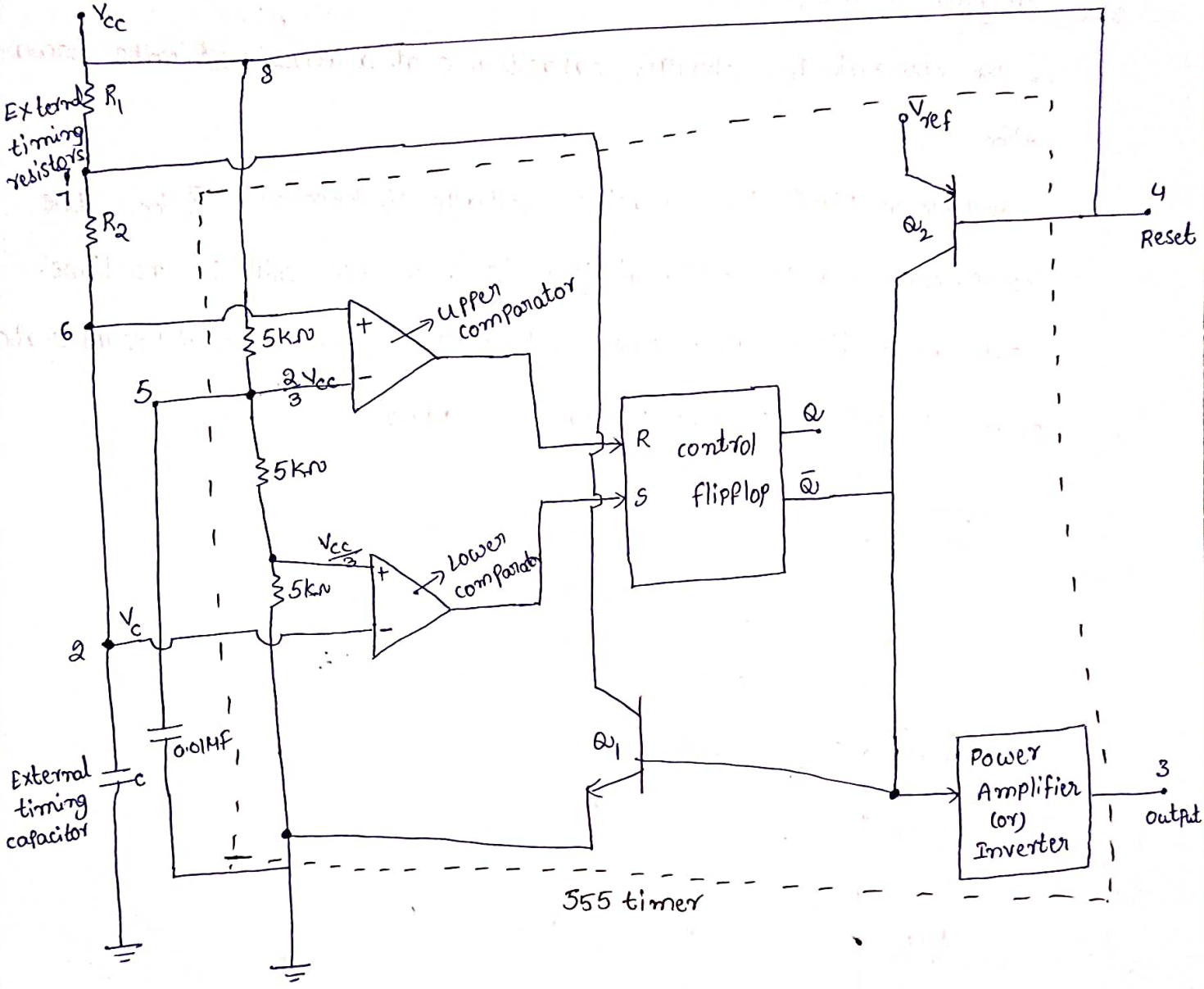
Time period, $T = \frac{V_{cc} \cdot C}{3 I_C}$ sec

I_C = charging current $= \frac{V_{cc} - V_D}{R} = \frac{V_{cc} - V_{BE}}{R}$

Therefore, frequency is

$$f = \frac{1}{T} = \frac{3I_c}{V_{cc} \cdot C} \text{ Hz}$$

Astable multivibrator using Ic 555 :-



This circuit has no stable state. The circuit changes its state alternately. Hence the operation is also called free running nonsinusoidal oscillator.

In case of Astable multivibrator, external timing resistor (R) is divided into 2 parts i.e R_1, R_2. The control pin (i.e Inverting terminal of upper comparator) is connected to ground through capacitor of 0.01MF. The Threshold pin (i.e Non Inverting terminal of upper comparator) and trigger pin (i.e Inverting terminal of lower comparat -or) are connected to V_{cc} terminal.

when power supply V_{cc} is ON, external timing capacitor starts charging towards V_{cc} at a rate of $(R_1+R_2)C$.

During charging period, output of upper comparator is Low, whereas the output of Lower comparator is High. Therefore, $\bar{Q}$ output is Low, hence output of timer is HIGH.

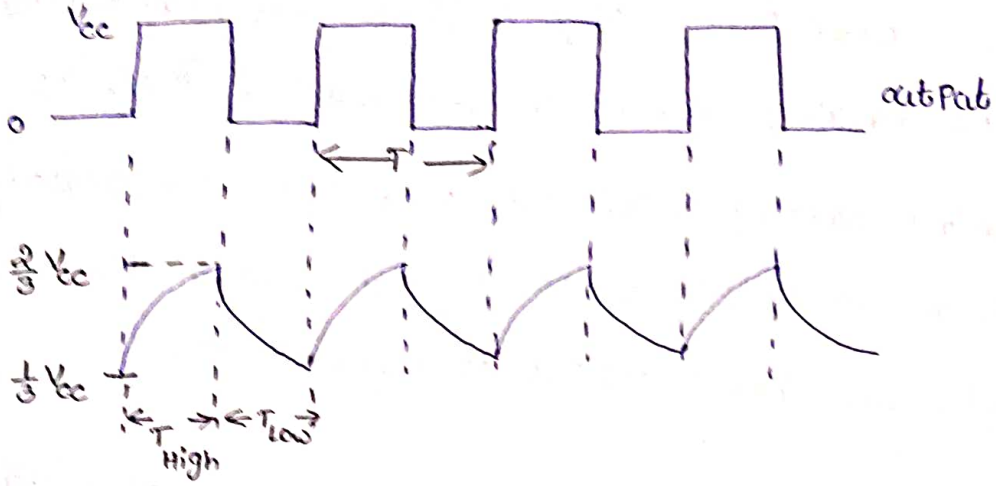
The voltage across capacitor becomes greater than upper threshold voltage i.e $\frac{2}{3}V_{cc}$, output of upper comparator is High, due to which output $\bar{Q}$ is High and output of timer becomes Low. Therefore, transistor Q_1 is switched ON, which in turn makes the capacitor to discharge at a rate of R_2C to 0V through R_2 and Q_1.

As soon as the voltage across capacitor becomes Lower than Lower threshold voltage i.e $\frac{1}{3}V_{cc}$, output of Lower comparator becomes Low, due to which output of $\bar{Q}$ is Low and output of timer becomes High.

This makes the Q_1 OFF and capacitor C gets unclamped.

Thus the capacitor charges to $\frac{2}{3}V_{cc}$ and discharges to $\frac{1}{3}V_{cc}$ periodically.

In this state of operation the output will be maintained at high for a period of time that is required for capacitor to charge from $\frac{1}{3}V_{cc}$ to $\frac{2}{3}V_{cc}$.



The voltage across the capacitor is given by

$$V_c = V_{cc}\,(1 - e^{-t/RC}) \quad -①$$

At $t = t_1$, capacitor charges from 0 to $\frac{2}{3}V_{cc}$

i.e $V_c = \frac{2}{3}V_{cc}$, $t = t_1$

eq ① $\Rightarrow$ $\frac{2}{3}V_{cc} = V_{cc}\,(1 - e^{-t_1/RC})$

$\Rightarrow \frac{2}{3} = 1 - e^{-t_1/RC}$

$\Rightarrow e^{-t_1/RC} = 1 - \frac{2}{3}$

$= \frac{1}{3}$

$\Rightarrow \frac{-t_1}{RC} = \ln\left(\frac{1}{3}\right)$

$$\Rightarrow t_1 = -Rc \ln\left(\frac{1}{3}\right)$$

$$\therefore t_1 = 1.09\,Rc \quad \text{—— (2)}$$

At time t_2, capacitor charge from 0 to $\frac{1}{3}V_{cc}$

i.e, $t = t_2$, $V_c = \frac{1}{3}V_{cc}$ eqn (1) becomes

$$\frac{1}{3}V_{cc} = V_{cc}\left(1 - e^{-t_2/Rc}\right)$$

$$\Rightarrow e^{-t_2/Rc} = 1 - \frac{1}{3}$$

$$= \frac{2}{3}$$

$$\Rightarrow t_2 = -Rc \ln(0.6)$$

$$\therefore t_2 = 0.405\,Rc \quad \text{—— (3)}$$

Therefore, time required by the capacitor to charge from $\frac{1}{3}V_{cc}$ to $\frac{2}{3}V_{cc}$ is,

$$t_{High} = t_1 - t_2$$

$$= 1.09Rc - 0.405\,Rc$$

$$= 0.69\,Rc$$

From circuit, $R = R_A + R_B$

$$\Rightarrow t_{High} = 0.69\,(R_A + R_B)C \quad \text{—— (4)}$$

The output is Low, capacitor discharges from $\frac{2}{3}V_{cc}$ to $\frac{1}{3}V_{cc}$, voltage across capacitor is given by,

$$\frac{1}{3}V_{cc} = \frac{2}{3}V_{cc}\, e^{-t/Rc}$$

$$\Rightarrow \frac{1}{2} = e^{-t/Rc}$$

$$\Rightarrow \ln\left(\frac{1}{2}\right) = -\frac{t}{Rc}$$

$$\Rightarrow -Rc \ln(2) = t$$

$$\Rightarrow \boxed{t = 0.69\,Rc} \quad \text{—— (5)}$$

From the circuit, $R = R_B$

$$\Rightarrow \boxed{t_L = 0.69 R_B C}$$

$\therefore$ Total time $(T) = t_{high} + t_{low}$

$$= 0.69 (R_A + R_B)C + 0.69 R_B C$$

$$\boxed{T = 0.69 (R_A + 2R_B) C} \quad \text{—⑥}$$

$$\therefore f = \frac{1}{T} = \frac{1.45}{(R_A + 2R_B)C} \quad \text{—⑦}$$

The Duty cycle of the circuit is defined as the ratio of ON time to the total Period of time.

$$\text{i.e} \quad D = \frac{t_{low}}{T} \times 100$$

$$\%D = \frac{R_B}{R_A + 2R_B} \times 100$$

If $R_A = R_B$, $\Rightarrow \%D = 33.33\%$.

If the output voltage high time is considered

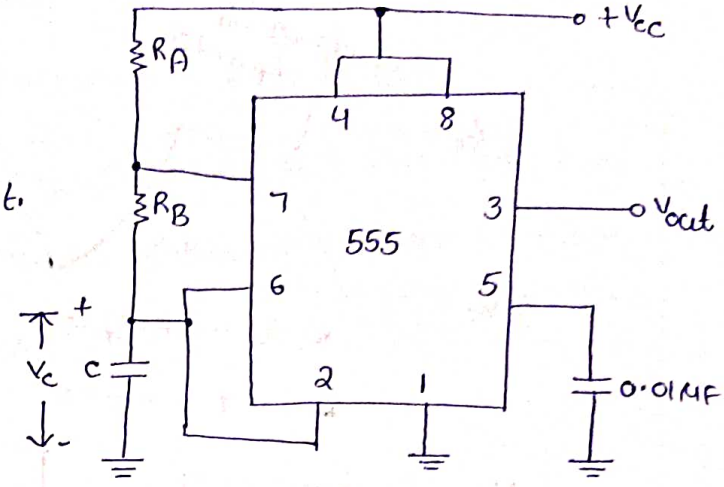
$$\%D = \frac{t_{high}}{T} \times 100$$

$$= \frac{R_A + R_B}{R_A + 2R_B} \times 100$$

If $R_A = R_B$, $\Rightarrow \%D = 66.67\%$.

→ If we need % duty cycle = 50% i.e $t_{high} = t_{low}$. For that if we make $R_A = 0$ then we will get 50%

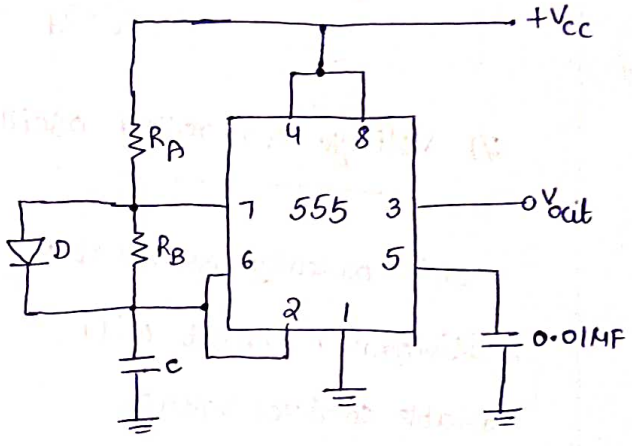
Schematic diagram :-



It shows the schematic diagram of Astable timer circuit. It contains R_A, R_B & C. Pin 4 is tied to Pin 8 & Pin 5 is grounded through a small capacitor.

Applications of Astable multivibrator :-

1. Square wave generator :-

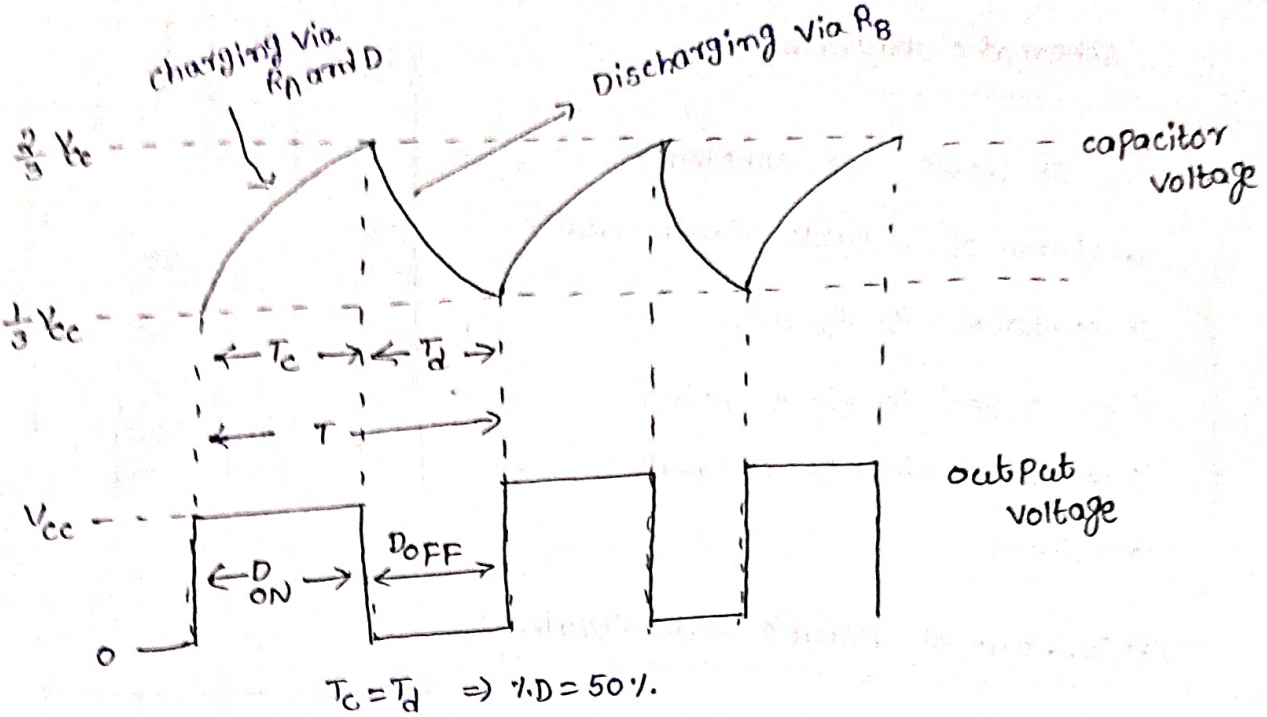


To observe expression of duty cycle, it is not possible to achieve 50% duty cycle.

To get exactly 50% duty cycle i.e square wave output is necessary to modify the Astable timer circuit

In modified circuit, capacitor C charges through R_A and diode D and discharges through R_B. To obtain square wave (50% duty cycle) resistance R_B is adjusted such that it is equal to summation of R_A and forward resistance of diode D. usually potentiometers used for a exact adjustments of resistors.

Waveforms :-



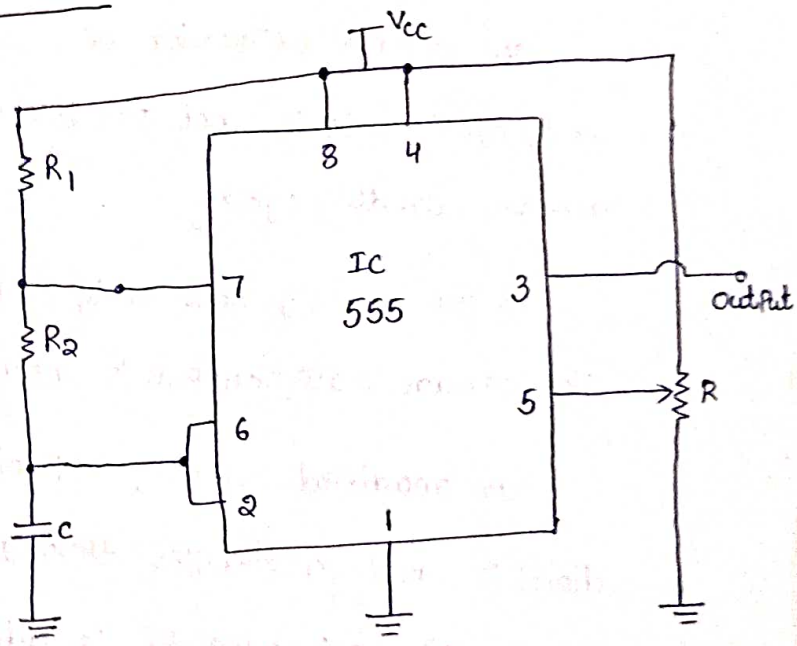
$T_c = T_d \Rightarrow \%D = 50\%$.

2) Voltage controlled oscillator (VCO) :-

It is basically an Astable multivibrator circuit with variable control voltage.

→ we know that, Internally control voltage is at $\frac{2}{3}V_{cc}$.

→ In this circuit control voltage is externally set by the potentiometer.

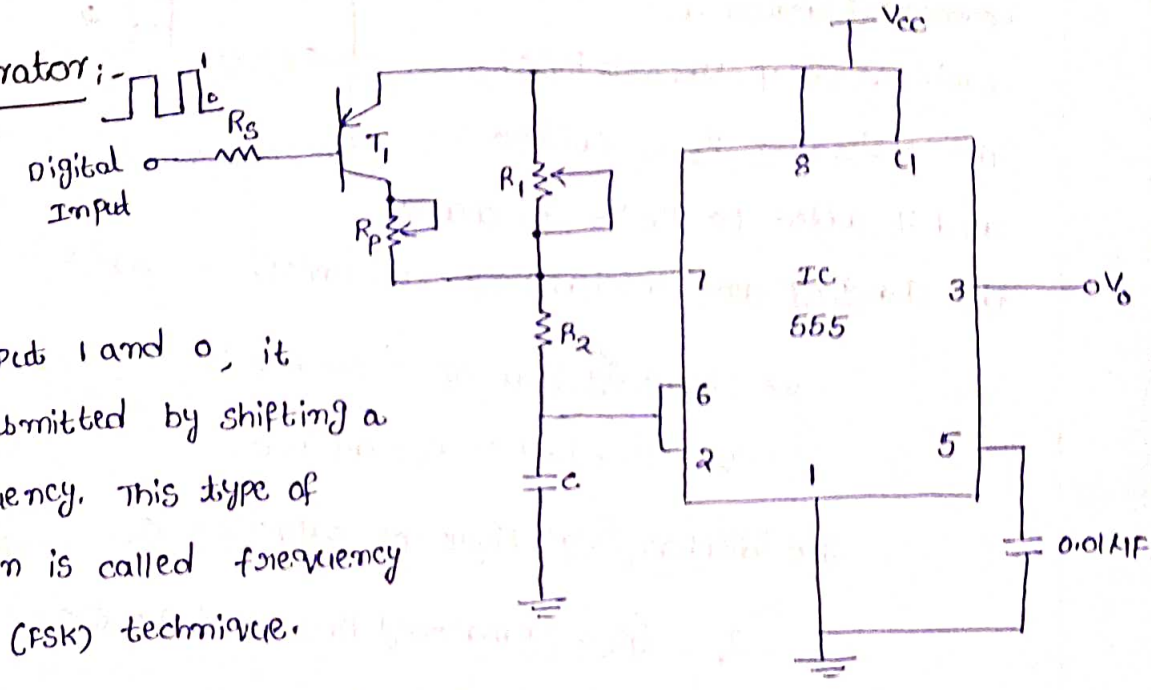


→ To change control voltage, upper threshold voltage changes and time required to charge capacitor upto upper threshold voltage changes. Similarly discharge time also changes. As a result, frequency of output voltage changes.

→ If control voltage is Increased, capacitor will take more time to charge and discharge and frequency will decrease.

→ If control voltage is decreased, capacitor will take less time to charge and discharge, it Increases frequency of output signal. So, varying control voltage, we can change the frequency.

3. FSK Generator:-



→ Binary Input 1 and 0, it can be transmitted by shifting a carrier frequency. This type of transmission is called frequency shift keying (FSK) technique.

→ when digital Input is High (logic 1), transistor T_1 OFF & 555 timer works in normal Astable mode.

The frequency of output waveform is

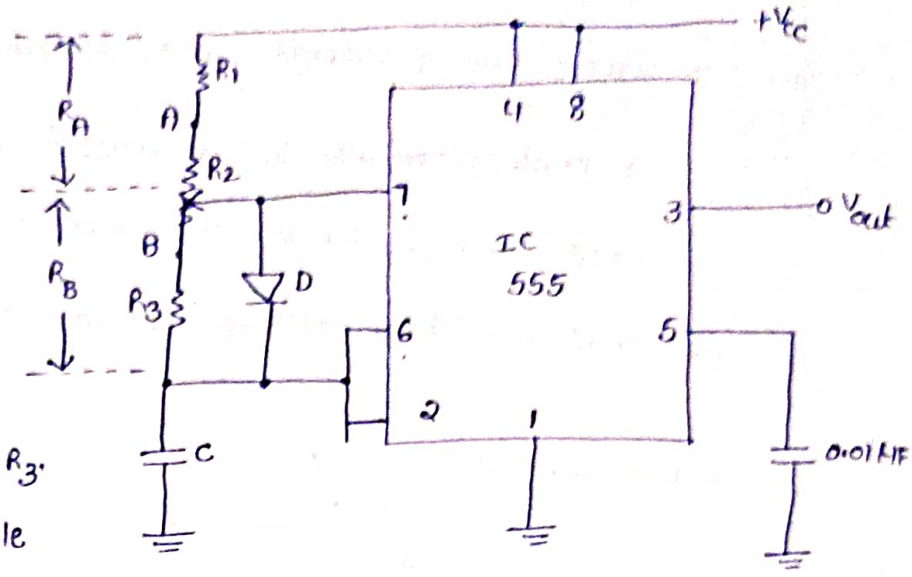
$$f_o = \frac{1.45}{(R_A + 2R_B)C} \quad (or) \quad \frac{1.45}{(R_1 + 2R_2)C}$$

→ when input is Low (logic 0), Transistor T_1 ON and it connects resistance R_P in Parallel with R_1.

The frequency of output is,

$$f_o = \frac{1.45}{[(R_1 \| R_P) + 2R_2]C}$$

4. Adjustable duty cycle :-



This circuit is similar to square wave generator, but instead of connecting diode across R_B it is connected across a combination of variable R_2 & R_3. The resistance R_2 is variable and it added to R_1, R_3 to change the charging and discharging resistance.

The charging time of capacitor is,

$$T_c = (R_1 + \text{Part of } R_2)\ 0.693\ C$$

The discharging time of capacitor is,

$$T_d = (R_3 + \text{remaining Part of } R_2)\ 0.693\ C$$

$$\therefore T = T_d + T_c = 0.693C\ [R_1 + R_2 + R_3]$$

$$f = \frac{1}{T} = \frac{1.44}{(R_1 + R_2 + R_3)C}$$

Let, Position of R_2 Potentiometer is A. i.e Part of R_2 in series with R_1 is zero & R_2 added to R_3

$$\therefore T_c = R_1\ 0.693C$$

$$\& \quad T_d = (R_2 + R_3)\ 0.693C$$

$$\therefore T = 0.693C\ [R_1 + R_2 + R_3]$$

No change in frequency but,

$$\%D_{min} = \frac{T_c}{T} \times 100 = \frac{0.693 R_1 C}{0.693 C (R_1+R_2+R_3)} \times 100$$

$$\boxed{\%D_{min} = \frac{R_1}{R_1+R_2+R_3} \times 100}$$

Thus min. duty cycle, less than 50% is possible.

FOR, R_2 Potentiometer position at B, max. duty cycle is possible

$$\therefore T_c = 0.693 (R_1+R_2) C$$

$$\& \quad T_d = 0.693 R_3 C$$

$$\therefore T = 0.693 (R_1+R_2+R_3) C$$

$$\therefore \%D_{max} = \frac{T_c}{T} \times 100 = \frac{0.693 (R_1+R_2) C}{0.693 (R_1+R_2+R_3) C} \times 100$$

$$\boxed{\%D_{max} = \frac{R_1+R_2}{R_1+R_2+R_3} \times 100}$$

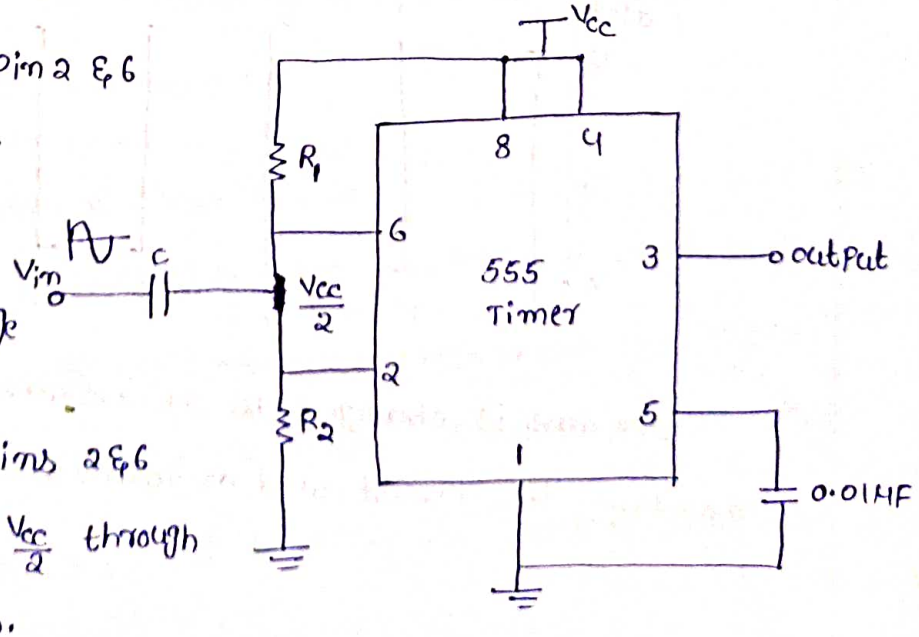
Schmitt trigger (or) 555 timer as a schmitt trigger :-

The Input is given to Pin 2 & 6 which are tied together.

Pins 4, 8 are connected to supply voltage (V_{cc}).

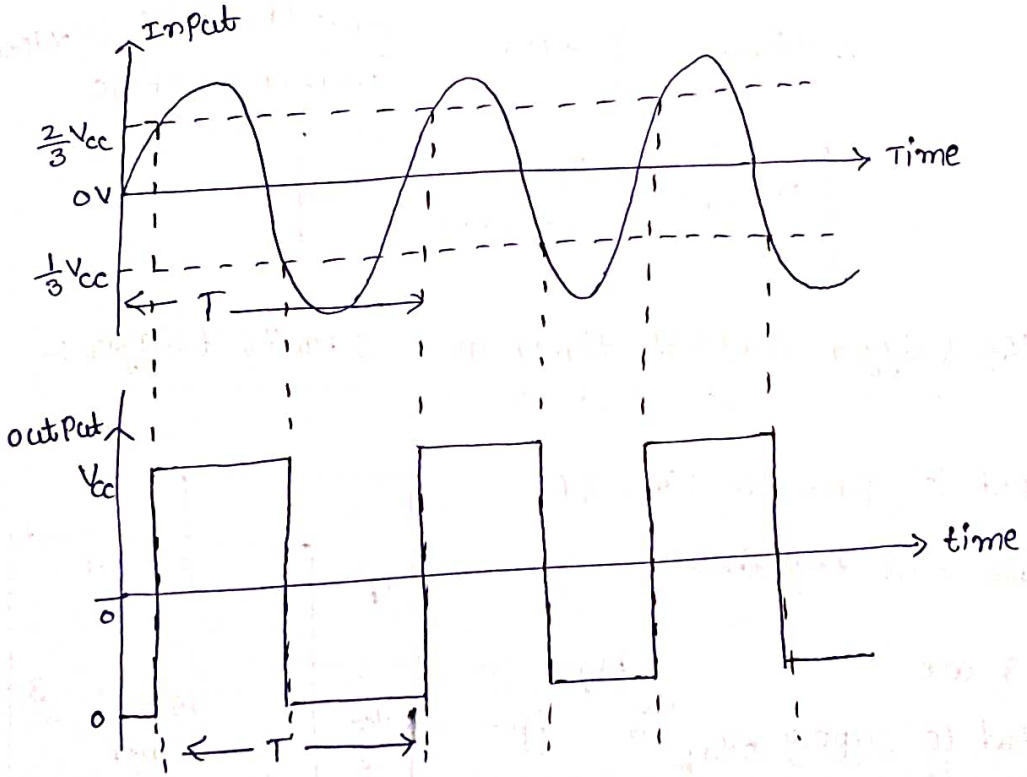
The common point of 2 Pins 2 & 6 is externally biased at $\frac{V_{cc}}{2}$ through resistance network R_1, R_2.

Generally, $R_1 = R_2$, to get biasing of $\frac{V_{cc}}{2}$.



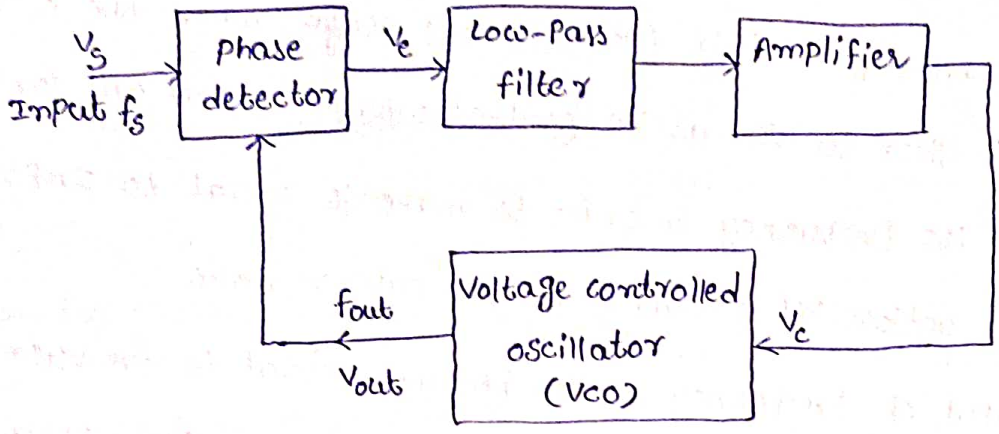
The upper comparator will trip at $\frac{2}{3}V_{cc}$ while lower comparator at $\frac{1}{3}V_{cc}$. The bias provided by R_1 and R_2 is centerd with in 2 thresholds.

when a sinusoidal wave whose Amplitude is greater than $\frac{2}{3}V_{cc} - \frac{1}{3}V_{cc}$ is applied to circuit, the comparators get triggered at reference level there by causing Internal control flip flop to set and reset alternatively. Due to this, square wave is generated at the output.



Sine wave is changed to square wave with out changing the frequency Therefore, this circuit used as wave shaping circuit.

Phase Locked Loop (PLL) :-



1. Phase detector (or) Phase comparator :-

When an Input voltage (V_S) of frequency f_S is applied to circuit, The phase comparator compares it output voltage V_0. If the frequency of two Incoming signals are different, it will generate difference signal, it also called error voltage. It contains output having both high frequency components ($f_S + f_{out}$) and low frequency components ($f_S - f_{out}$). This error output is applied to low pass filter.

2. Low pass filter :- The output of phase detector is given to Input of LPF. It contains both high frequency components and low frequency components, LPF allows only low frequency components and reject all high frequency components. So, the output of low pass filter (LPF) contains only ($f_S - f_{out}$) signals and it applied to Input of Amplifier.

3. Amplifier :- The output of low pass filter is given to Input of Amplifier. It is used to amplifies the signal and given to VCO.

→ It Amplifies the error voltage, it also called as error Amplifier.

4. Voltage controlled oscillator (Vco):-

Initially PLL is in free running state. when the output of Amplifier is given to Vco as its control voltage, based on control voltage Vco shifts its frequency in order to make it equal to Input frequency. During this action PLL is said to be in "capture mode."

→ The output of frequency of Vco becomes equal to frequency of Input signal, $f_{in} - f_{out} = 0$. In this condition PLL is said to be in "Locked mode".

In Locked mode PLL, tracks the frequency of Input signal. This cycle repeats and PLL tracks the changes in Input frequency.

Important definitions related to PLL:-

1. Lock-in range:- once the PLL is locked, it can track frequency changes in the incoming signal. The range of frequencies over which the PLL can maintain lock with the Incoming signals is called "Lock range" (or) "tracking range."

2. capture range:-

The range of frequencies over which the PLL can acquire Lock with an Input signal is called "capture range".

3. Pull-in time:- The total time taken by the PLL to establish a lock is called Pull-in time.

Individual blocks in PLL :-

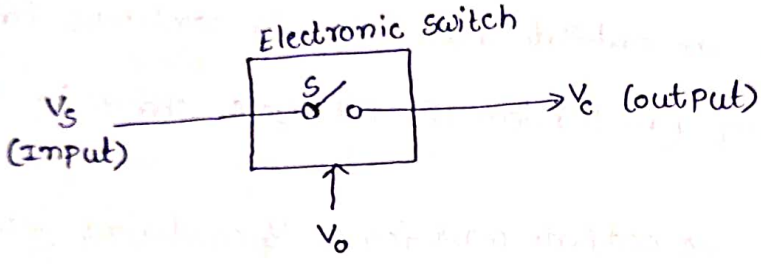
1. Phase detector / comparator :-

There are 2 types of phase detectors

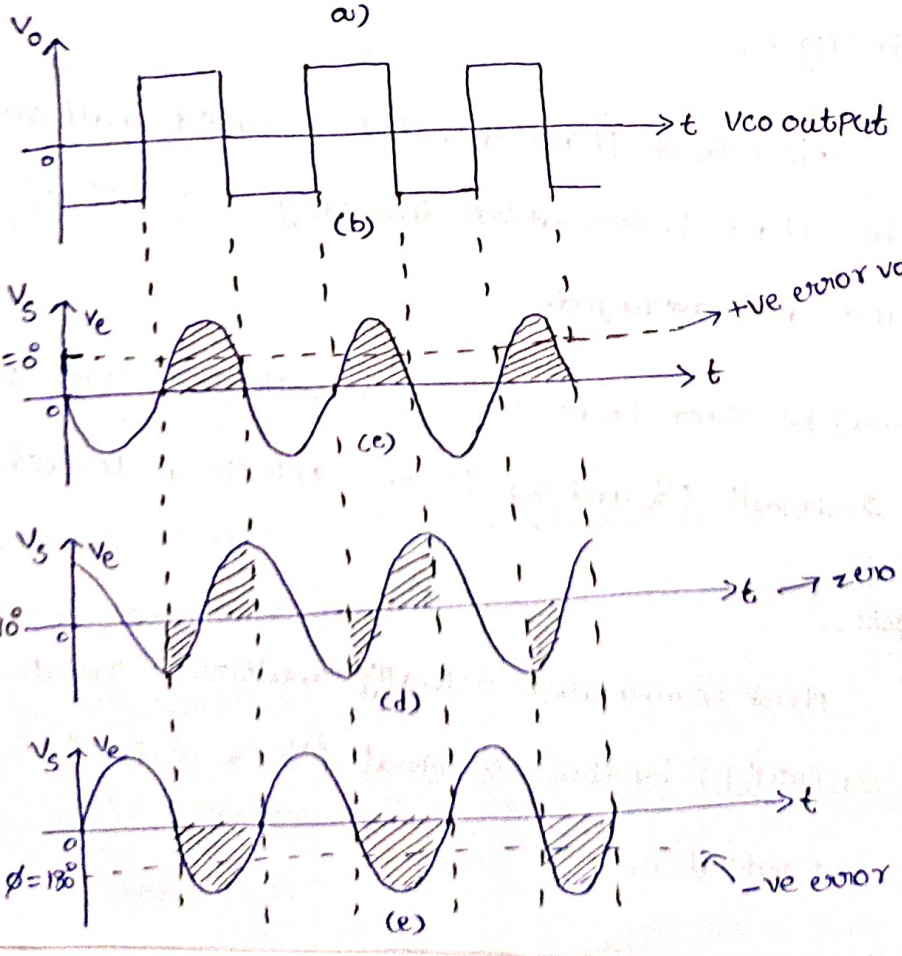
1. Analog phase detector
2. Digital phase detector

1. Analog phase detector :- There are 2 types i.e 1. Switch type
2. Balanced modulator type

i) Switch type phase detector :-



a)



above fig. shows basic circuit and waveforms of Analog phase detector.

→ Switch 'S' is opened & closed by signal coming from Vco.

The switch is closed when Vco output is +ve otherwise it is open.

i) when $\phi = 0^\circ$:-

when switch 'S' is closed only when Vco output is +ve, the output wave form V_e will be half sinusoids (shaded Portion) shown in fig 'c'.

ii) when $\phi = 90^\circ$:- The output waveform V_e contains half portion of negative cycle and half portion of +ve cycle shown in fig 'd'.

iii) when $\phi = 180^\circ$:- The output waveform V_e contains -ve half sinusoids shown in fig 'e'.

This type of phase detector is called half wave detector, since the phase information for only one half of Input waveform is detected and averaged.

→ It may be seen that the error voltage is zero when phase shift between 2-Inputs (V_s and V_o) is 90°, this is a perfect lock condition.

Analysis :-

phase comparator actually multiplies Input signal ($V_s = V_s \sin(2\pi f_s t)$ by the Vco signal ($V_o = V_o \sin(2\pi f_o t + \phi)$).

The output is

$$V_e = K V_s V_o \sin(2\pi f_s t) \sin(2\pi f_o t + \phi) \quad -①$$

where,

$K \rightarrow$ constant

$\phi \rightarrow$ phase shift between Input signal and Vco output

$$\Rightarrow V_e = \frac{K V_s V_o}{2} [\cos(2\pi f_s t - 2\pi f_o t - \phi) - \cos(2\pi f_s t + 2\pi f_o t + \phi)] \quad -②$$

At lock condition, $f_s = f_o$

$$V_e = \frac{K V_s V_o}{2} [\cos(-\phi) - \cos(2\pi \times 2 f_o t + \phi)] \quad -③$$

eq③, shows phase detector output contains double frequency term and d.c term.

The d.c term $\frac{K V_s V_o}{2} \cos\phi$ varies as a function of phase ϕ, i.e $\cos\phi$ between 2 signals.

The double frequency term is filtered by LPF and d.c term is applied to modulating input terminal of Vco. The dc term ie dc error voltage is zero at $\phi = 90°$. Therefore, perfect lock condition $f_s = f_o$ and $\phi = 90°$.

Problems associated with switch type phase detector :-

1. The output voltage V_e is proportional to Input signal amplitude V_s. This is undesirable since it makes phase detector gain and loop gain dependent on Input signal amplitude.

2. The output is proportional to $\cos\phi$ and not proportional to ϕ making it Non-linear.

2. Balanced modulator type phase detector;-

The Problems in switch type phase detector can be eliminated by making amplitude of Input signal constant. This can be achieved by converting sinusoidal Input signal into square wave Input signal.

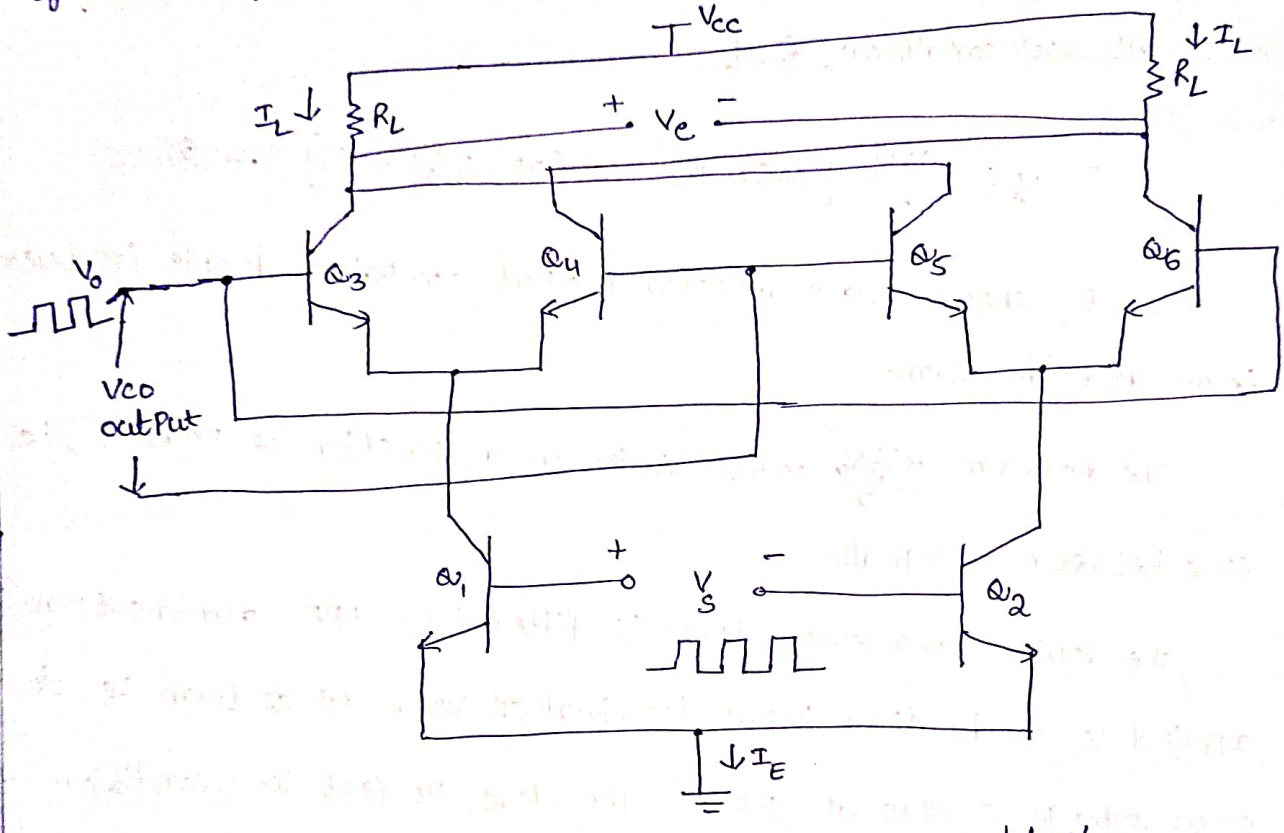


Fig:- Balanced modulator type phase detector

The Input signal is applied to differential Pair Q_1Q_2. Transistors Q_3-Q_4 and Q_5-Q_6 are 2 sets of SPDT (single pole double through) switches activated by Vco output.

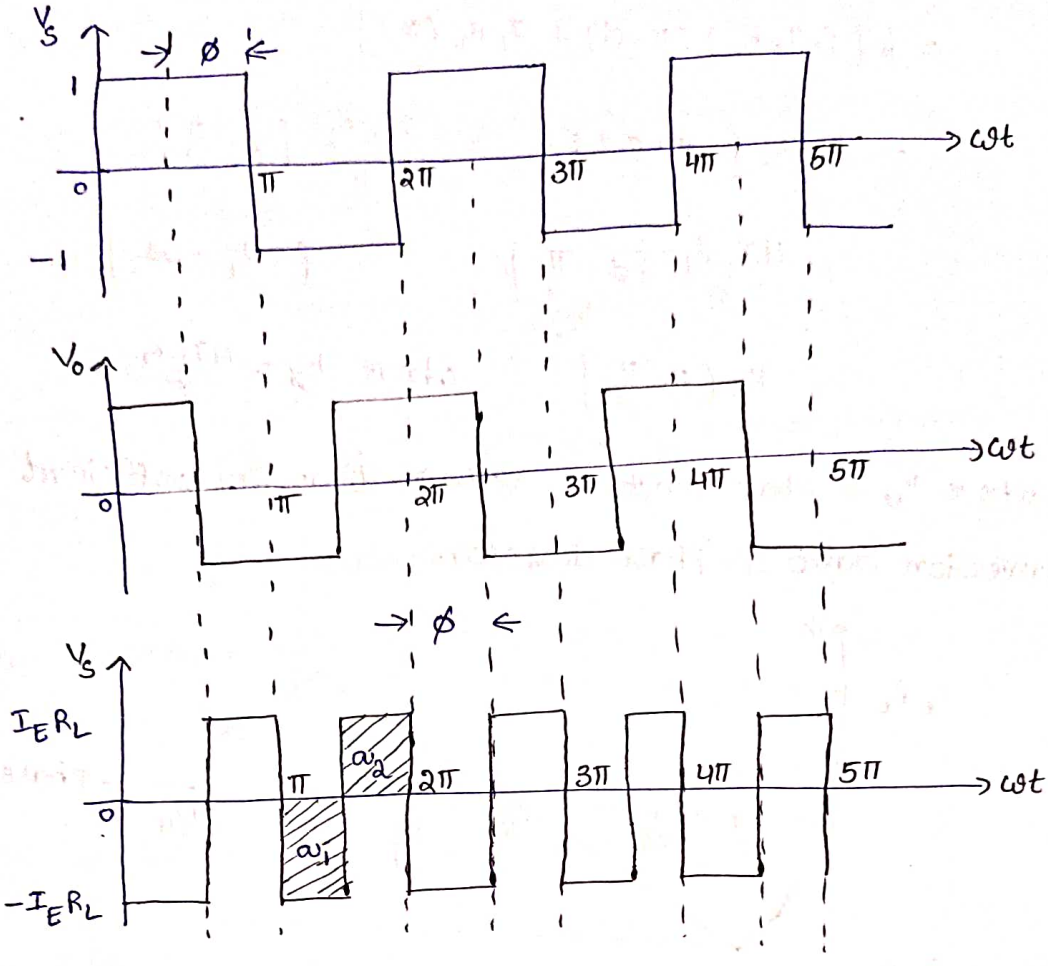


Fig:- wave forms of Balanced modulator Phase detector

when V_s is +ve, ~~Q_1~~ Q_1 ON and Q_2 OFF. when V_o is +ve $Q_3, Q_6 \rightarrow$ ON $Q_4, Q_5 \rightarrow$ OFF.

when V_s is -ve, Q_1 OFF, Q_2 ON . when V_o is -ve $Q_3, Q_6 \rightarrow$ OFF $Q_4, Q_5 \rightarrow$ ON.

The output error voltage is given by

$$V_e = I_E R_L .$$

The average value of phase detector output V_e can be calculated as,

$$(V_e)_{avg} = \frac{1}{\pi}[(\text{area } A_1) + (\text{area } A_2)]$$

$$= \frac{1}{\pi}\left[(-I_E R_L)(\pi-\phi) + I_E R_L(\phi)\right]$$

$$= \frac{I_E R_L}{\pi}\left[-\pi+\phi+\phi\right] = \frac{2I_E R_L}{\pi}\left[\phi-\frac{\pi}{2}\right]$$

$$= \frac{4I_L R_L}{\pi}\left[\phi-\frac{\pi}{2}\right] \qquad [\because I_E = 2I_L]$$

$$= K_\phi\left(\phi-\frac{\pi}{2}\right] \qquad \text{where } K_\phi = \frac{4I_L R_L}{\pi}$$

where K_ϕ → Phase angle-to- voltage transfer coefficient (or) conversion ratio of phase detector.

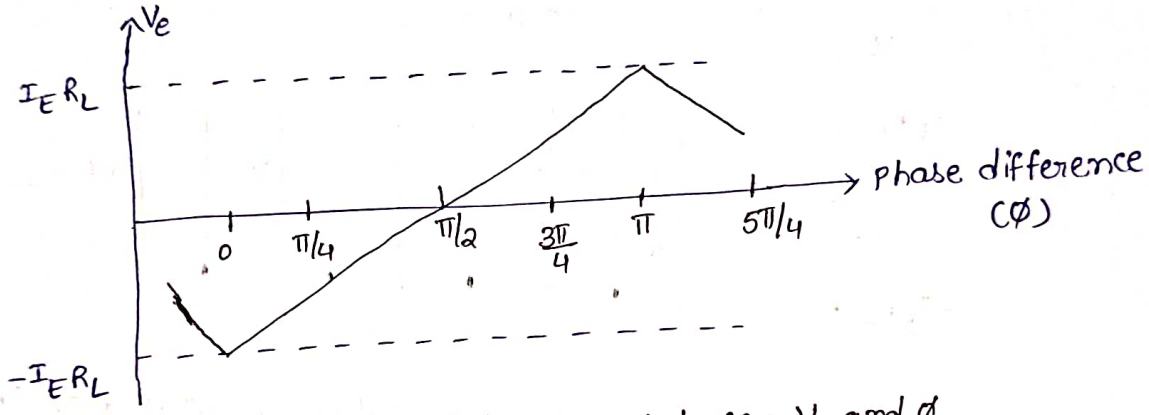
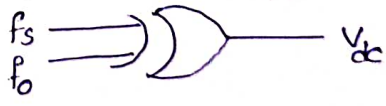


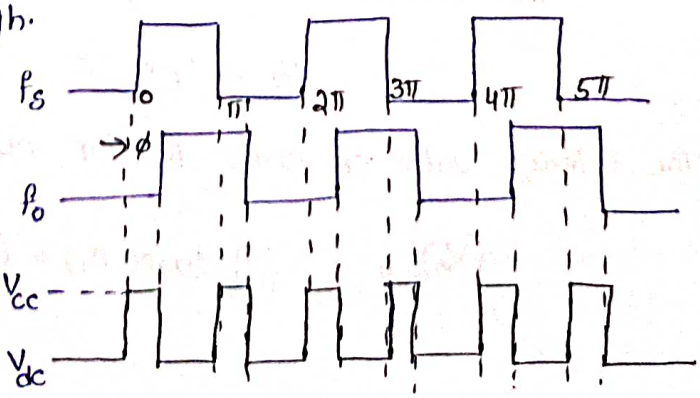
Fig:- Relation ship between V_e and ϕ

2. Digital Phase detector :-

The XOR gate can be used as a digital phase detector when both signal f_s and f_o are square waves.



The output of XOR gate is high when only one of the Input is high.



Input/output waveforms

According to waveform, f_s is leading f_o by ϕ degrees.

From fig, when $\phi = 0$, $V_{dc} = 0$ and when $\phi = \pi$, $V_{dc} = V_{cc}$.

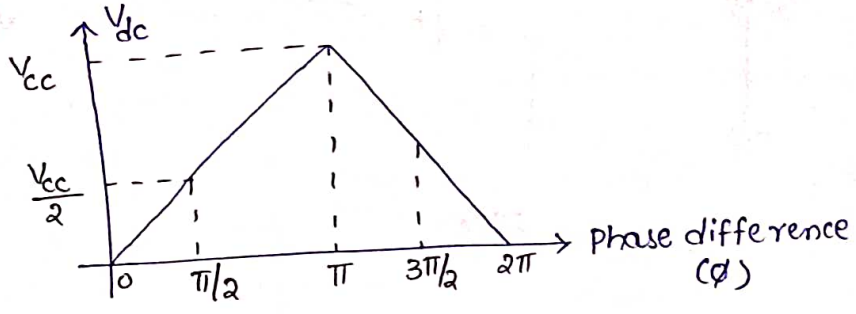


Fig :- Relation ship between V_{dc} and ϕ

The conversion ratio K_ϕ for a supply voltage V_{cc} is:

$$K_\phi = \frac{V_{cc}}{\pi}$$

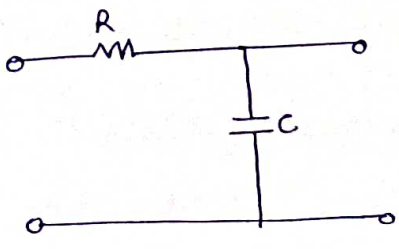
If $V_{cc} = 5V$, $K_\phi = 5/\pi = 1.591$ V/rad.

Low Pass filter :-

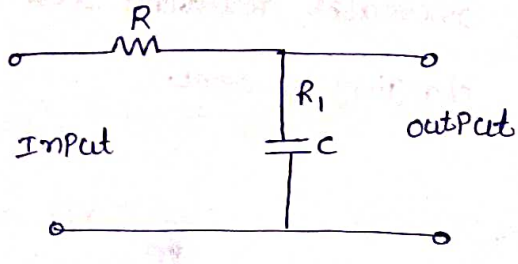
The Low Pass filter not only removes high frequency components and noise, but also controls the dynamic characteristics of PLL. These characteristics Include capture range, lock range, Bandwidth, transient response.

If filter band width is reduced, response time increases. Bandwidth of filter reduces, reducing capture range of PLL.

The filters may be either passive (or) active type



a) LPF



b) Passive filter

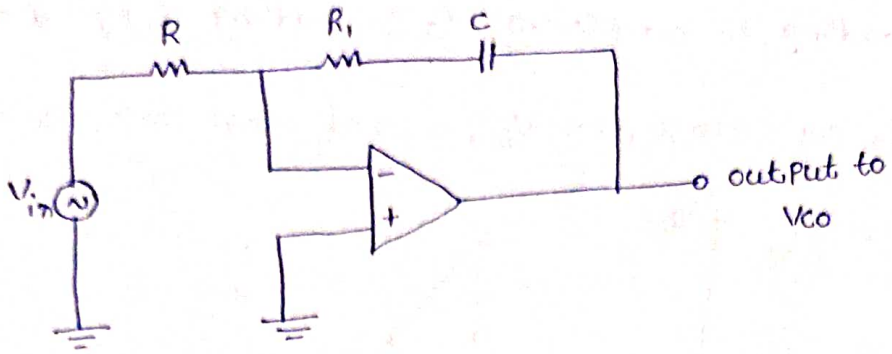


Fig:- Active filter

Voltage controlled oscillator (VCO) :-

A common type of VCO available in IC form is NE/SE 566.

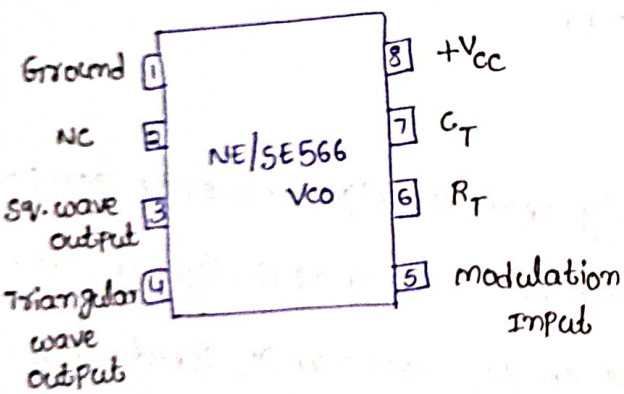


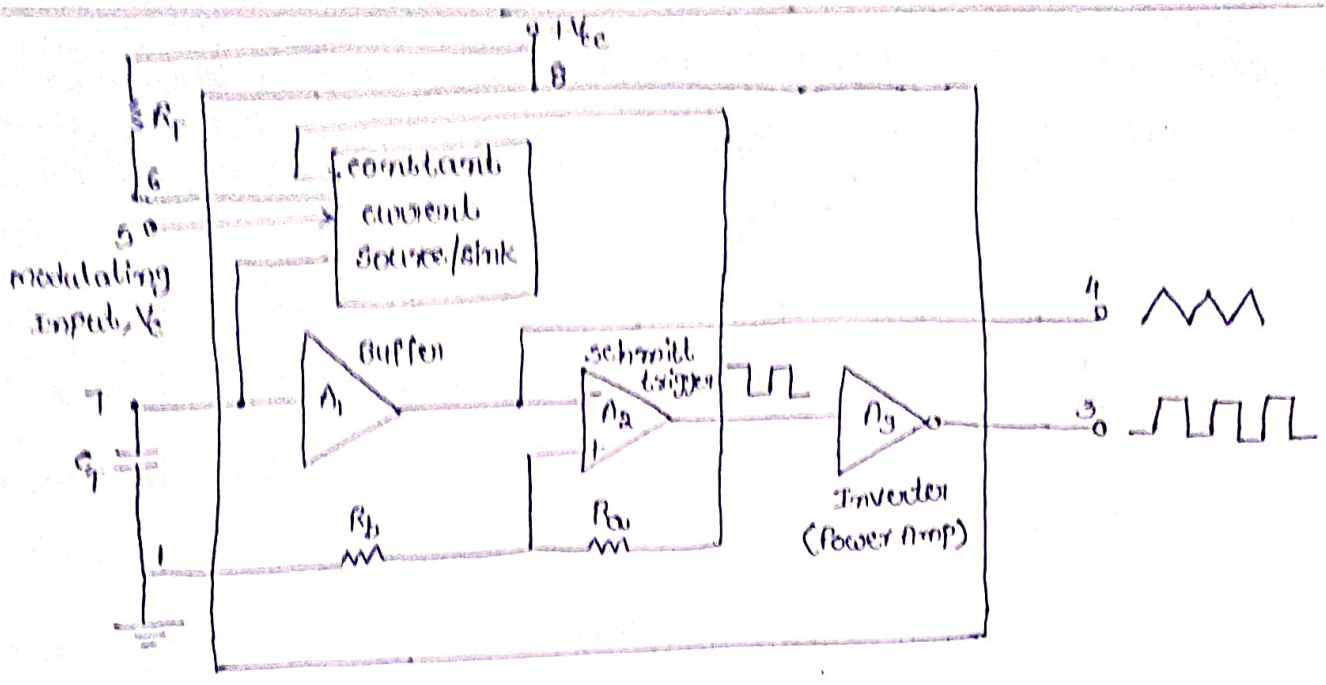
Fig:- Pin-configuration

→ Timing capacitor C_T is linearly charged (or) discharged by constant current source/sink.

→ The amount of current can be controlled by changing V_c applied at modulating Input (Pin 5) (or) changing timing resistor R_T external to IC chip.

→ The voltage at Pin 5 is held same voltage as Pin 6.

→ If modulating voltage at Pin 5 is increased, voltage at Pin 6 also increases, resulting less voltage across R_T thereby decreasing charging current.



→ A small capacitor 0.001μF should be connected between pin 5 and 6 to eliminate possible oscillations.

→ The voltage across C_T is applied to Inverting terminal of schmitt trigger A_2 via buffer Amplifier A_1.

→ The voltage across schmitt trigger is designed to V_{cc} and $0.5V_{cc}$.

If $R_A = R_B$ in +ve feed back loop, voltage at non-inverting terminal of A_2 swings from $0.5V_{cc}$ to $0.25V_{cc}$.

→ The voltage on capacitor C_T exceeds $0.5V_{cc}$ during charging, the output of schmitt trigger goes Low ($0.5V_{cc}$).

→ Now capacitor discharges when it at $0.25V_{cc}$, the output of schmitt trigger goes High (V_{cc}).

→ we get triangular waveform across C_T which is available at Pin4.

→ Inverted square wave output is available at Pin 3.

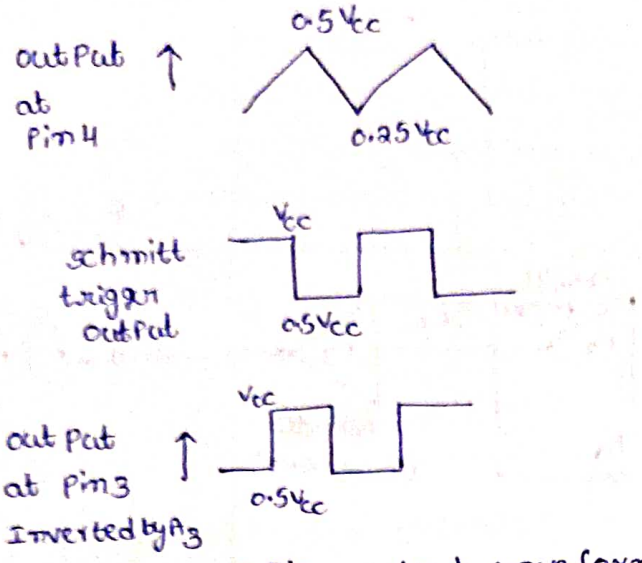


Fig :- output waveform

The output frequency of VCO can be calculated as

The total voltage on capacitor changes from 0.25 V_{cc} to 0.5 V_{cc}.

So, $\Delta V = 0.25\, V_{cc}$.

$$\frac{\Delta V}{\Delta t} = \frac{i}{C_T}$$

$$\frac{0.25\, V_{cc}}{\Delta t} = \frac{i}{C_T}$$

$$\Rightarrow \Delta t = \frac{0.25\, V_{cc}\, C_T}{i} \quad \text{---} ①$$

Total Time period of triangular waveform = $2\Delta t$.

frequency of oscillator $f_o = \frac{1}{T} = \frac{1}{2\Delta t}$

$$= \frac{i}{0.5\, V_{cc}\, C_T} \quad \text{---} ②$$

But $i = \frac{V_{cc} - V_c}{R_T}$

$$\Rightarrow f_o = \frac{2(V_{cc} - V_c)}{V_{cc}\, C_T\, R_T} \quad \text{---} ③$$

The output frequency of Vco can be changed either by i) R_T ii) C_T iii) The voltage V_c at modulating input terminal Pin5.

→ modulating Input voltage is varied from 0.75 V_{cc} to V_{cc} which can produce a frequency variation about 1 to 1.

→ with no modulating input signal, voltage at Pin 5 is biased at $(\frac{7}{8})V_{cc}$

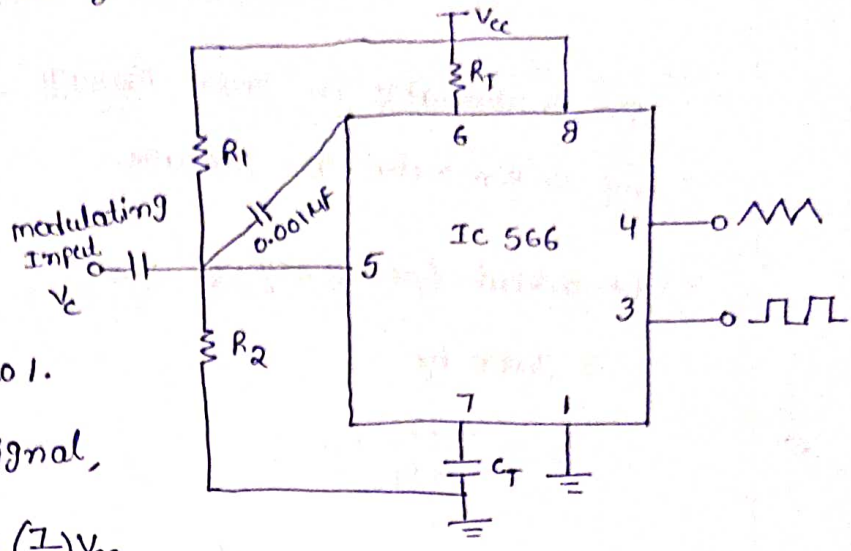


Fig:- Pin configuration for Vco.

$$\Rightarrow f_o = \frac{2(V_{cc} - (7/8)V_{cc})}{V_{cc} R_T C_T} = \frac{1}{4 R_T C_T} = \frac{0.25}{R_T C_T} \quad \text{—— (4)}$$

Voltage to frequency conversion factor (K_V):-

$$K_V = \frac{\Delta f_o}{\Delta V_c} \quad \text{—— (5)}$$

ΔV_c → modulation voltage required to produce the frequency shift Δf_o for a Vco.

$$\Delta f_o = f_1 - f_o = \frac{2(V_{cc} - V_c + \Delta V_c)}{R_T C_T V_{cc}} - \frac{2(V_{cc} - V_c)}{R_T C_T V_{cc}} = \frac{2\Delta V_c}{R_T C_T V_{cc}}$$

$$\Rightarrow \Delta V_c = \frac{\Delta f_o R_T C_T V_{cc}}{2} \quad \text{—— (6)}$$

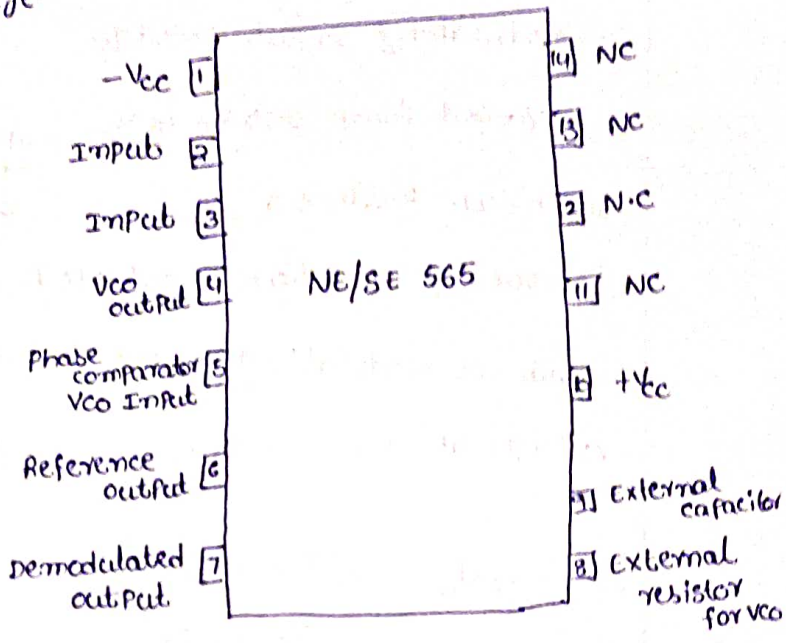
Put value of $R_T C_T$ from eq (4),

$$\Delta V_c = \Delta f_o V_{cc} / 8 f_o$$

$$\text{(or)} \quad K_V = \frac{\Delta f_o}{\Delta V_c} = \frac{8 f_o}{V_{cc}} \quad \text{—— (5)}$$

Functional diagram of 565 (or) Internal block diagram of 565 :-

565 is available in 14-DIP Package and 10-Pin metal can Package.



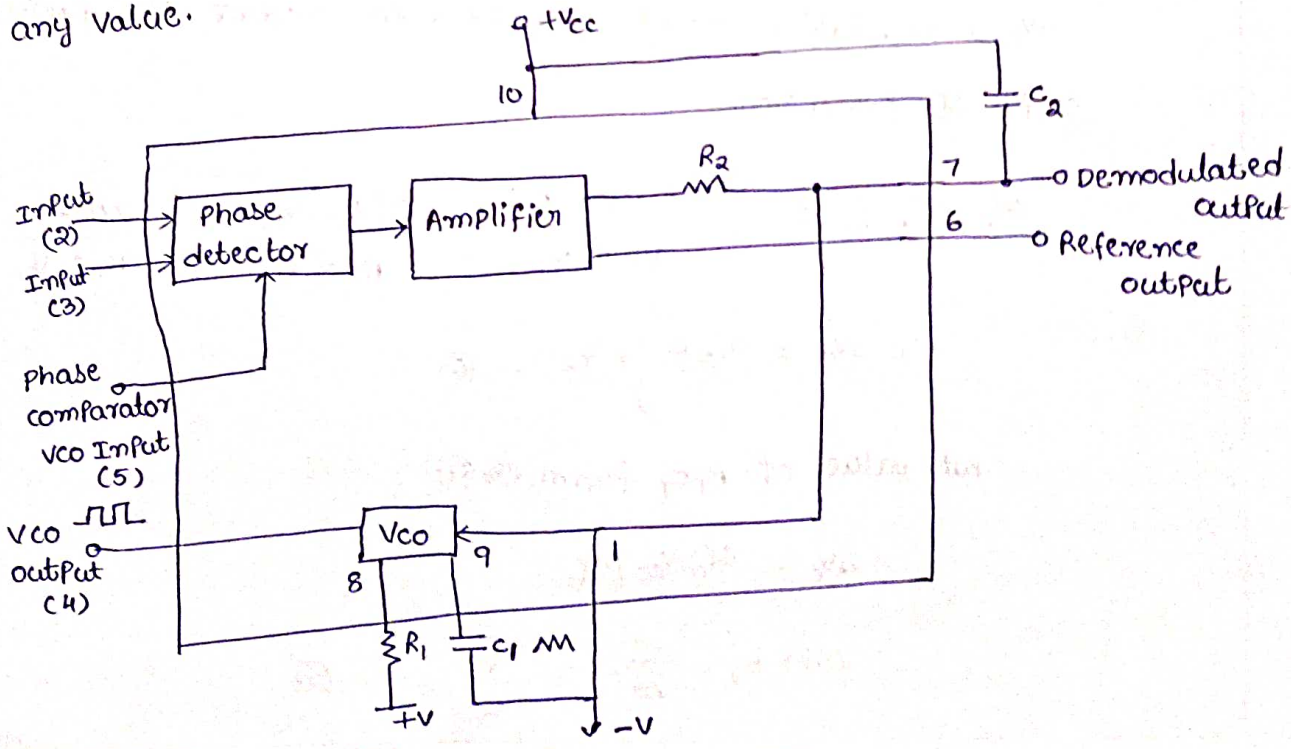
The output frequency of VCO is given by

$$f_0 = \frac{0.25}{R_T C_T} \text{ Hz.}$$

where R_T, C_T are External resistor and capacitor connected to Pin 8, 9.

The values of R_T, C_T are adjusted such that free running freq. will be at center of Input frequency range.

The value of R_T is restricted from 2KΩ to 20KΩ, capacitor have any value.



→ capacitor C_2 connected between pin 7 and +ve supply (Pin 10) forms 1st order Low Pass filter with Internal resistance of 3.6KΩ

→ The value of C_2 should be large enough to eliminate possible oscillations in Vco voltage.

The Lock range and capture range for IC565 PLL are given by

$$f_L = \pm \frac{8 f_o}{V} \text{ Hz}$$

and $$f_c = \pm \left[\frac{f_L}{2\pi (3.6)(10^3) C_2} \right]^{1/2}$$

Derivation of Lock-in range :-

If ϕ radians is the phase detector difference between analog signal and Vco voltage, The output voltage of phase detector is

$$V_e = K_\phi (\phi - \pi/2) \quad \text{—①}$$

$K_\phi \rightarrow$ Phase angle-to-voltage transfer coefficient

The control voltage is,

$$V_c = A K_\phi (\phi - \pi/2) \quad \text{—②}$$

$A \rightarrow$ Gain

V_c shifts Vco frequency from its free running frequency f_o to frequency f,

$$f = f_o + K_V V_c \quad \text{—③}$$

$K_V \rightarrow$ voltage to frequency transfer coefficient

PLL is Locked into signal frequency f_s,

$$f = f_s = f_o + K_V V_c$$

$$V_c = (f_s - f_o)/K_V = A K_\phi (\phi - \pi/2)$$

$\Rightarrow A K_\phi (\phi - \pi/2) = (f_s - f_0)/K_v$

$(\phi - \pi/2) = (f_s - f_0)/K_v A K_\phi$

$\Rightarrow \phi = \frac{\pi}{2} + (f_s - f_0)/K_v A K_\phi$

max. output voltage magnitude available from phase detector occurs for $\phi = \pi$, $V_{c(max)} = \pm K_\phi \frac{\pi}{2}$

$(f - f_0)_{max} = K_v V_{c(max)}$

$V_{c(max)} = \pm \frac{\pi}{2} K_\phi A$

max. VCO frequency swing that can be obtained

$(f - f_0)_{max} = K_v V_{c(max)}$

$= K_v K_\phi A(\pi/2)$

max. range of signal frequency over which PLL can remain locked

$f_s = f_0 \pm (f - f_0)_{max}$

$= f_0 \pm K_v K_\phi (\pi/2) A$

$= f_0 \pm \Delta f_L$

$2\Delta f_L$ will be lock-in- freq. range

$2\Delta f_L = K_v K_\phi A\pi$

$\Delta f_L = \pm K_v K_\phi A(\pi/2)$

Free running frequency f_0,

$K_v = \frac{8 f_0}{V}$

$V = V_{cc} - (-V_{cc})$

$K\phi = \frac{1.4}{\pi}$

$A = 1.4$

Lock-In-range, $\Delta f_L = \pm 7.8\ f_o/V$

$$\boxed{\Delta f_L = \pm \frac{7.8}{V} f_o}$$

Derivation of capture range:-

The phase angle difference between the signal and vco output voltage will be

$$\phi = (\omega_s t + \theta_s) - (\omega_o t + \theta_o) = (\omega_s - \omega_o)t + \Delta\theta \qquad [\because \Delta\theta = \theta_s - \theta_o]$$

Phase angle difference does not maintain constant it will be change with time at a rate given by

$$\frac{d\phi}{dt} = \omega_s - \omega_o$$

$$\therefore \Delta f = f_s - f_o$$

Low Pass filter is a simple Rc Network having

$$T(jf) = \frac{1}{1 + j(f/f_1)}$$

where $f_1 = \frac{1}{2\pi RC}$ is the 3-dB Point of LPF. slope position of LPF where $(f/f_1)^2 >> 1$

$$T(f) \simeq \frac{f_1}{jf} \Rightarrow T(\Delta f) \simeq \frac{f_1}{\Delta f}$$

The fundamental frequency term supplied to LPF by the phase detector will be difference frequency $\Delta f = f_s - f_o$

The voltage V_c to drive the VCO is,

$$V_c = V_\phi \times T(f) \times A$$

$$V_{c(max)} = V_{\phi(max)} \times T(f) \times A$$

$$= \pm K_\phi (\pi/2) A (f_1/\Delta f)$$

The corresponding value of max. VCO frequency shift is,

$$(f - f_0)_{max} = K_V V_{c(max)}$$

$$= \pm K_\phi K_V (\pi/2) A (f_1/\Delta f)$$

At $f = f_s$, max. signal frequency range,

$$(f_s - f_0)_{max} = \pm K_V K_\phi (\pi/2) A (f_1/\Delta f_c)$$

Now $\Delta f_c = (f_s - f_0)_{max}$

$$(\Delta f_c)^2 = K_V K_\phi (\pi/2) A f_1$$

$$\Delta f_L = \pm K_V K_\phi (\pi/2) A$$

wegel, $(\Delta f_c) \simeq \pm \sqrt{f_1 \Delta f_L}$

Total captwie range is, $2\Delta f_c \simeq 2\sqrt{f_1 \Delta f_L}$

$$\text{Lock-In-range} = 2\Delta f_L$$

$$= K_V K_\phi A \pi$$

$$(\Delta f_c)^2 = \Delta f_L \times f_1$$

$$\Delta f_c = \sqrt{\Delta f_L \times f_1}$$

$$f_1 = \frac{1}{2\pi R_1 C_1}$$

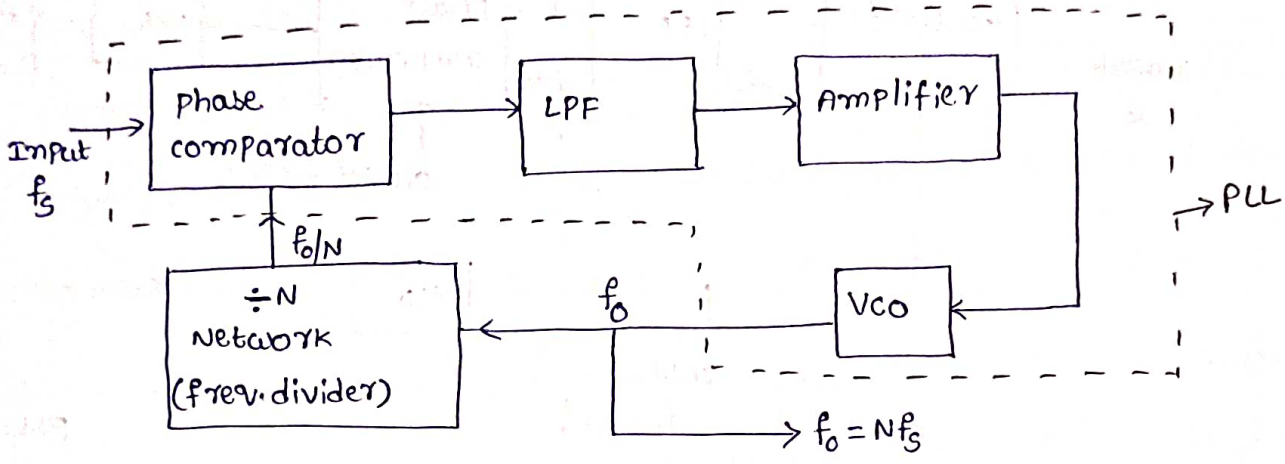
$$\Delta f_c = \sqrt{\frac{\Delta f_L}{2\pi R_1 C_1}} \Rightarrow \Delta f_c = \left(\frac{\Delta f_L}{2\pi R_1 C_1}\right)^{1/2}$$

In 565 PLL, $R_1 = 3.6\,k\Omega$

$$\Rightarrow \Delta f_C = \left[\frac{\Delta f_L}{2\pi \times 3.6 \times 10^3 \times C_1} \right]^{1/2}$$

Applications of PLL :-

1. Frequency multiplier / division :-



In this arrangement uses a divided by N Network between Vco output and phase comparator.

i) when PLL is in locked mode, In this condition output of frequency divider is same as the Input frequency f_s. Therefore, Vco output is multiple of f_{in}.

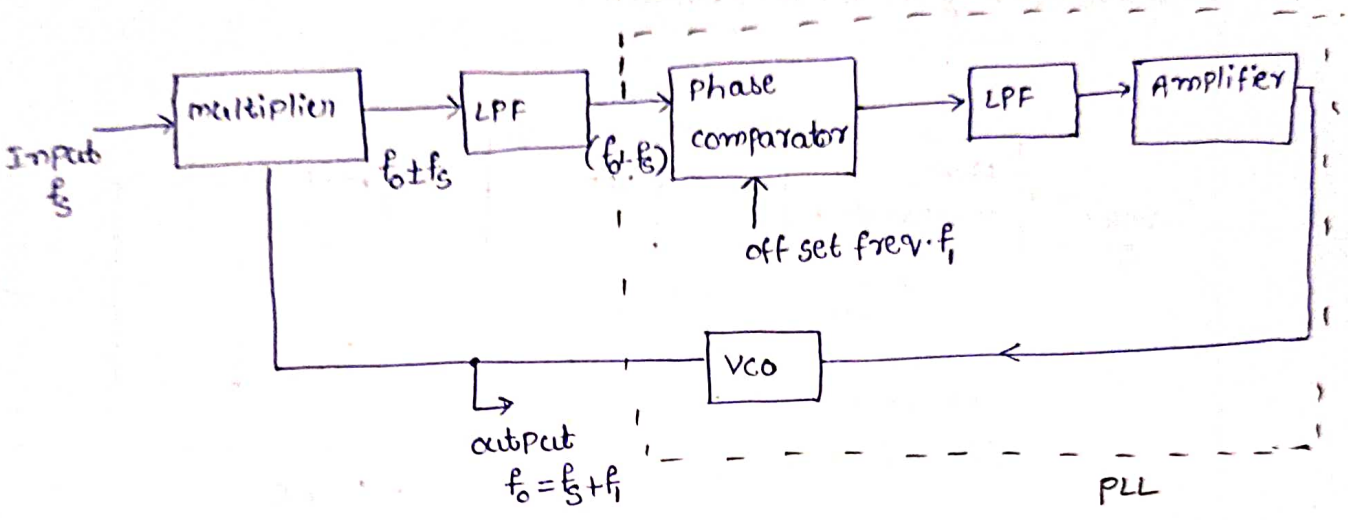
$$f_{out} = Nf_{in} \qquad N \rightarrow \text{Integer} \qquad (\text{or})\ f_{out} = Nf_s$$

ii) when PLL is in harmonic locking mode, If the Input signals are rich in harmonics e.g. square wave, pulse train etc.. then Vco can be locked directly to n^{th} harmonic of Input. As the Amplitude of higher harmonics decreases with Increase of order, The order (or) value of n is maintained below 10.

Frequency division obtained by locking m^{th} order harmonic of VCO output. since it is rich in harmonics.

The output $f_o = \frac{f_{in}}{m}$ (or) $f_o = \frac{f_s}{m}$

2) Frequency Translation:-



Input signal f_s and VCO output frequency f_{out} applied to multiplier. It has 2 Inputs and output is $f_{out} \pm f_s$. This output of multiplier is applied to LPF. It allows only low frequencies and rejects high frequency so output of LPF will be $f_o - f_{in}$.

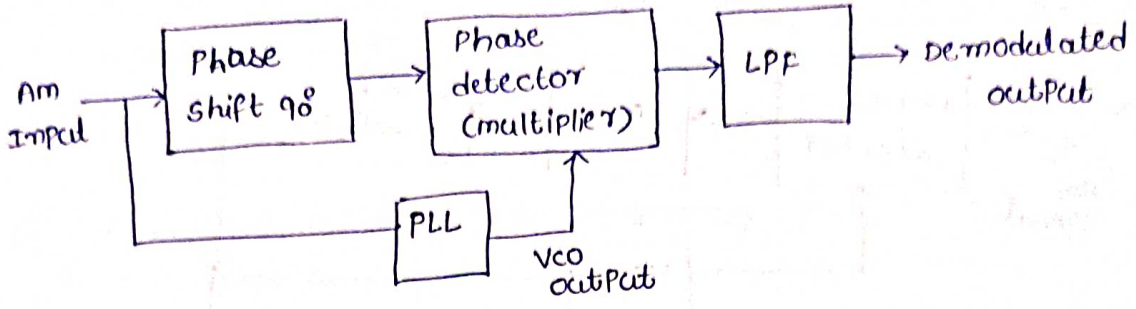
In locked state of PLL,

$$f_{out} = f_{in} = f \quad \text{(or)}$$

$$f = f_{out} - f_s$$

$$\Rightarrow \boxed{f_{out} = f + f_s}$$

3. Am detection (or) Am demodulator :-



when an Am signal is applied to circuit, PLL gets Locked to the carrier frequency of Am signal, and Vco present inside the PLL produces a signal whose frequency is same as the carrier of Am signal. Thus the Vco output of PLL is applied to multiplier.

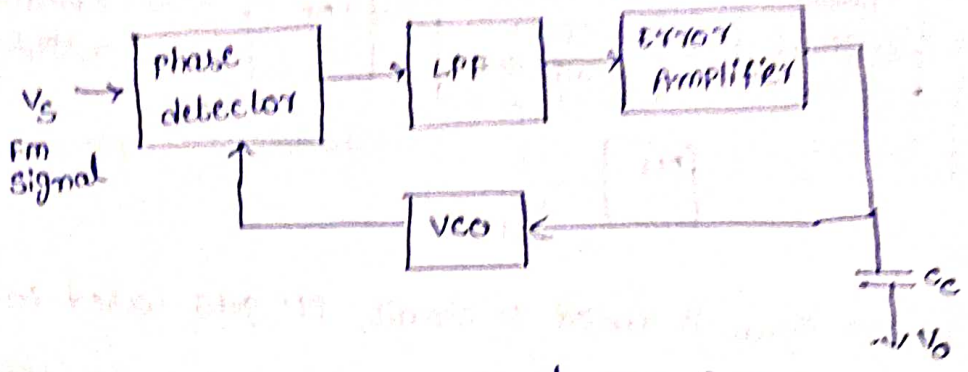
when Am signal passes through phase shift circuit, the phase shift of signal changes by 90°, since under locked state of PLL, output of Vco will be 90° outof phase with Input. The phase shifted signal applied to multiplier. The 2 signals applied to multiplier are in same phase. The output of multiplier given to LPF, which rejects high frequency components and passes only Low frequency components. The signal obtained at output of filter is demodulated output.

→ Am demodulator using PLL has

i) High degree of selectivity

ii) High degree of Noise immunity.

4. Fm demodulation:-



When PLL is Locked in Fm signal, Vco frequency follows the Instantaneous frequency of the Fm signal, and error voltage (or) Vco control voltage is proportional to deviation of Input frequency from the center frequency. Therefore, ac component of error voltage (or) control voltage of Vco will represent true replica of modulating voltage that is applied to Fm carrier at transmitter. The faithful reproduction of modulating voltage depends on linearity between Instantaneous frequency deviation and control voltage of Vco.

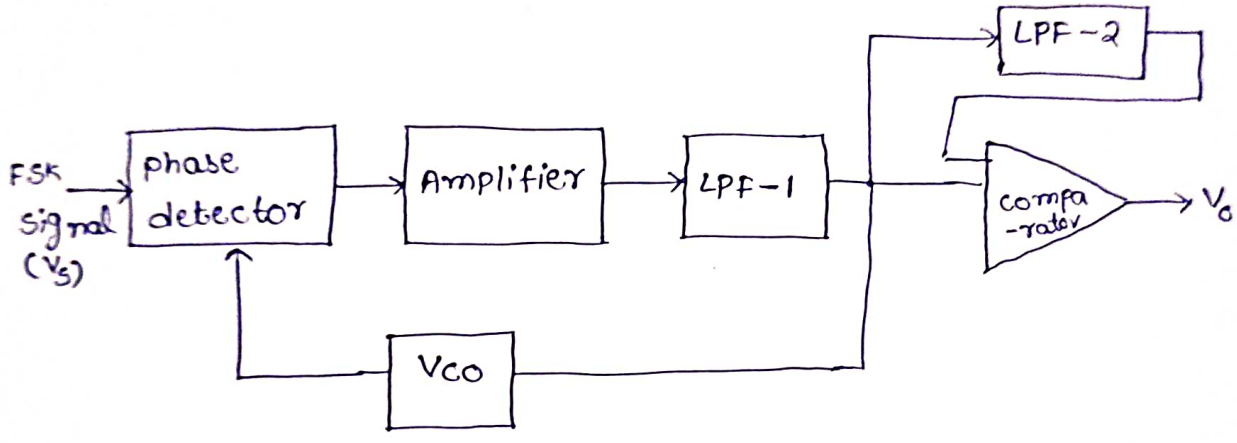
Note that Fm frequency deviation and modulating frequency should remain in Locking range of PLL to get faithful replica of modulating signal.

If the Product of modulation freq. f_m and freq. deviation exceeds $(\Delta f_c)^2$, Vco will not be able to follow the Instantaneous freq. Variations of Fm signal.

5 Frequency shift keying (FSK) demodulator :-

Binary data transmitted by means of carrier frequency. It uses 2 carrier frequencies Logic 0 (or) Logic 1. This type of data transmission is called frequency shift keying.

In this data transmission, on receiving end, 2 carrier frequencies are converted into 1 and 0 to get original data. This process is called FSK demodulation.



Let us consider 2 frequencies, 1-freq. respresents as '0' another freq. as '1'. If PLL remain in locked into FSK signal at both f_1, f_2 Vco control voltage which is also supplied to the comparator will given as

$$V_{c1} = (f_1 - f_0)/K_V$$

& $$V_{c2} = (f_2 - f_0)/K_V$$

where $K_V \rightarrow$ voltage to frequency transfer coefficient.

The difference between 2 control voltage levels will be

$$\Delta V_C = (f_2 - f_1)/k_v$$

The reference voltage for comparator is derived from additional lowpass filter and it is adjusted midway between V_{c1}, V_{c2}.

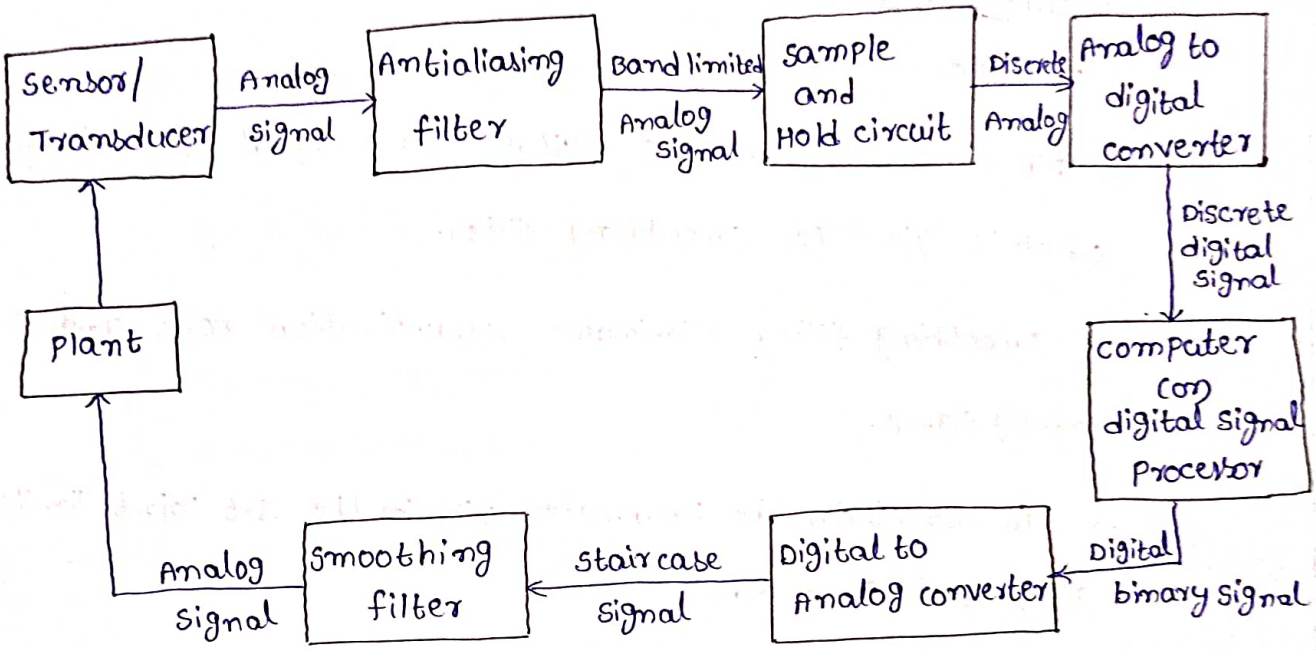
Therefore, V_{c1}, V_{c2} comparator gives output as '0' and '1'.

G. Venkata Hanuman
Asst. Prof

6. A/D and D/A converters

Introduction:-

Basic blocks Preceding an A/D and D/A converters :-



→ sensor/Transducer measures different physical Parameters such as temperature, Pressure, Voltage, current etc.. and provides output in Analog form.

→ The output of sensor is applied to Antialiasing filter. In this section, high frequency Noise signals are eliminated only Low frequency output is passed to sample and Hold circuit.

→ The function of sample and Hold circuit is to sample the output of filter at frequency which is greater than twice the maximum frequency of its inputs. and maintain constant value during Process of Analog to digital conversion.

→ The ADC converts sample and signal to its digital equivalent signal which is displayed on monitor of controlling system in which a control algorithm is loaded.

→ control Algorithm measures (or) compares the measured value with set value.

→ D/A converter converts digital binary signal to stair case signal which is given to smoothing filter.

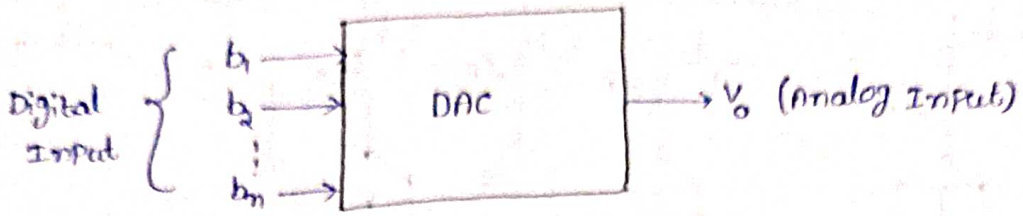
→ smoothing filter eliminates Quantization noise and Produces Analog signal.

→ To maintain the Parameter with in the set Point limits and to get output from plant.

Applications :-

1. Digital and Audio recording and playback
2. music and Video synthesis
3. Direct digital control
4. Data Acquistion
5. Digital signal Processing
6. Pulse code modulation
7. Digital multimeter
8. micro Processor based Instrumentation

D/A converters :-



$b_1 \rightarrow$ most significant bit (MSB) & $b_n \rightarrow$ Least significant bit (LSB)

mathematically,

$$V_o = K V_{FS} (b_1 2^{-1} + b_2 2^{-2} + \cdots + b_n 2^{-n})$$

where, $V_o \rightarrow$ output voltage

$K \rightarrow$ scaling factor usually it is unity

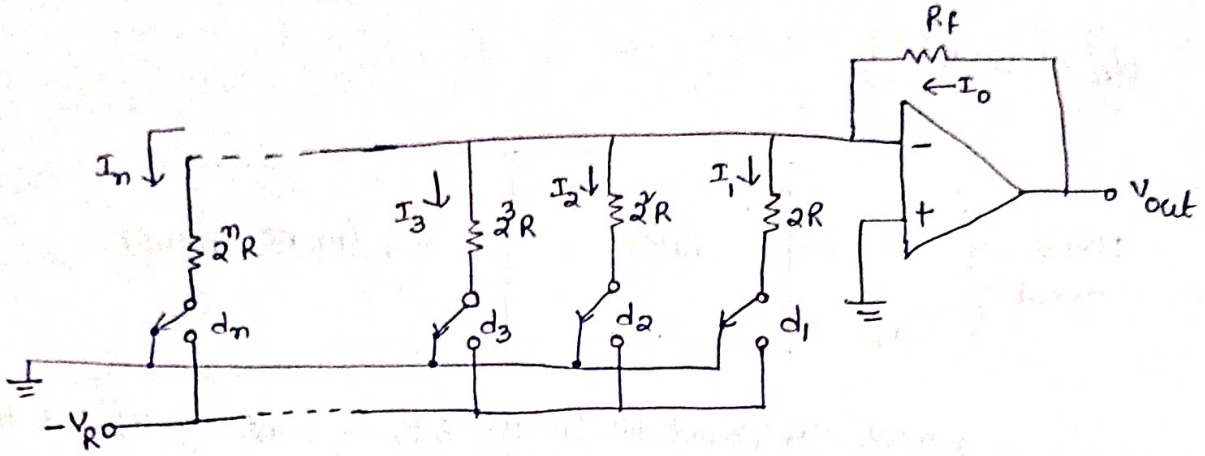
$V_{FS} \rightarrow$ Full scale output voltage.

D/A conversion techniques :-

1. weighted resistor method (or) Binary weighted resistor D/A converter
2. R-2R Ladder Network method
3. Inverted R-2R Ladder Network method
4. multiplying DAC (IC 1408)

1. Binary weighted Resistor D/A converter :-

A Binary weighted resistor DAC consists of Binary weighted resistor Network ($2R, 2^2R, 2^3R \cdots 2^nR$), summing Amplifier (either connected in Inverting mode (or) Non Inverting mode) and n-electronic switches ($d_1, d_2, d_3, \cdots d_n$).



From the figure, switch positions are controlled by digital Inputs.

* when digital Input is '1', ~~correspondi~~ switch is connected to reference voltage.
* when Input is '0', switch & resistor is connected to Ground.

Switch ON → $I = \frac{V_{ref}}{R}$

Switch OFF → $I = 0$.

Here, OP-Amp is used for Summing Amplifier,

The output current of OP-Amp is given by

$$I_{out} = I_1 + I_2 + I_3 + ---- + I_n$$

The output voltage across R_f is given by

$$V_o = -I_o R_f$$

$$= -[I_1 + I_2 + I_3 + ---- + I_n] R_f$$

$$= -\left[\frac{V_{ref}}{2R} d_1 + \frac{V_{ref}}{2^2 R} d_2 + \frac{V_{ref}}{2^3 R} d_3 + ---- + \frac{V_{ref}}{2^n R} d_n\right] R_f$$

$$= -V_{ref}\left[\frac{d_1}{2R} + \frac{d_2}{2^2R} + \frac{d_3}{2^3R} + \text{-----} + \frac{d_n}{2^nR}\right] R_f$$

$$= -V_{ref} \cdot \frac{R_f}{R}\left[\frac{d_1}{2} + \frac{d_2}{2^2} + \frac{d_3}{2^3} + \text{--} + \frac{d_n}{2^n}\right]$$

If $R_f = R$,

$$V_0 = -V_{ref}\left[\frac{d_1}{2} + \frac{d_2}{2^2} + \frac{d_3}{2^3} + \text{-----} + \frac{d_n}{2^n}\right]$$

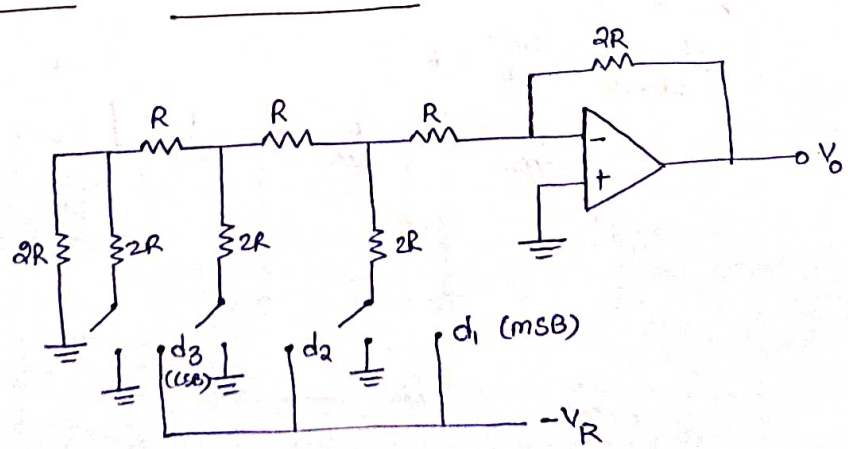
$$\boxed{V_0 = -V_{ref}\left[d_1 \bar{2}^1 + d_2 \bar{2}^2 + d_3 \bar{2}^3 + \text{-----} + d_n \bar{2}^n\right]}$$

From above equation, it is clear that Analog output voltage is directly proportional to Input binary (digital) word.

Draw backs:-

It requires wide range of binary weighted resistors. As no. of bits increases, required range of resistors also increases. i.e it does not used for more than 8-bits.

2. R-2R Ladder DAC (voltage Switched) :-



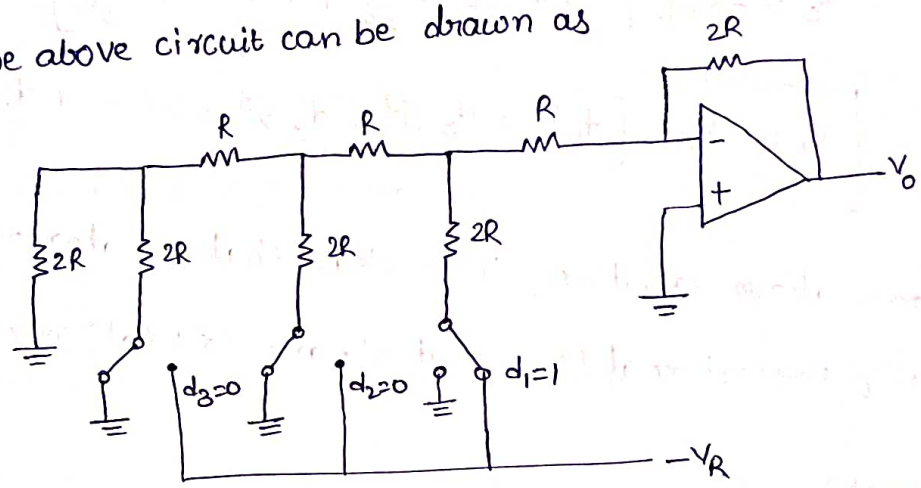
* It uses the resistors as R and 2R.

* In this circuit R → Resistors are connected in series & 2R resistors are connected in Parallel.

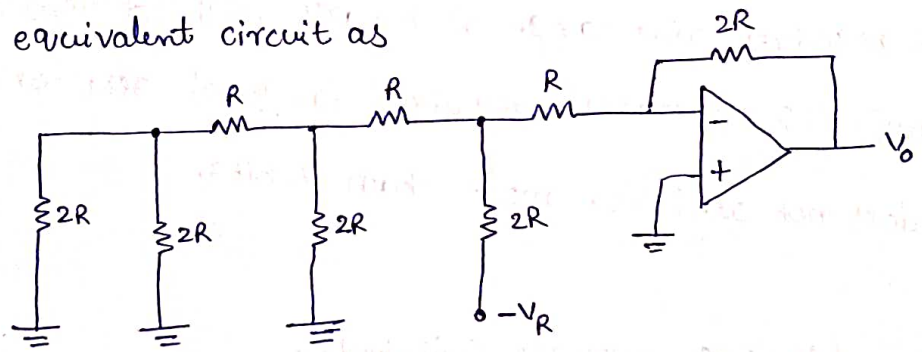
Ex:- consider 3-bit DAC as 100

$d_1=1,\ d_2=0,\ d_3=0$

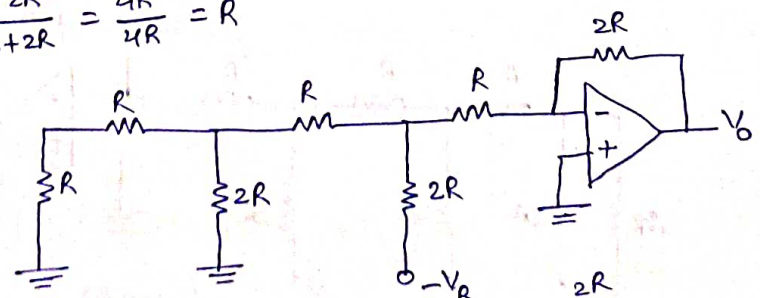
The above circuit can be drawn as

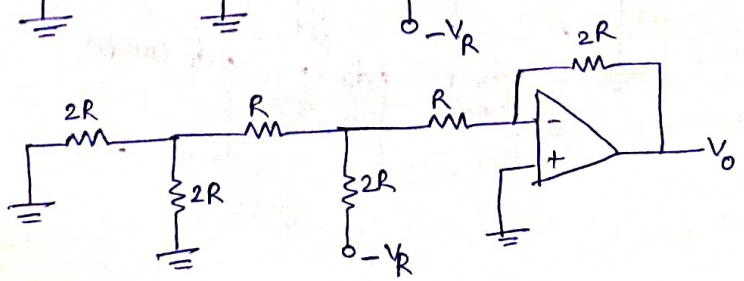


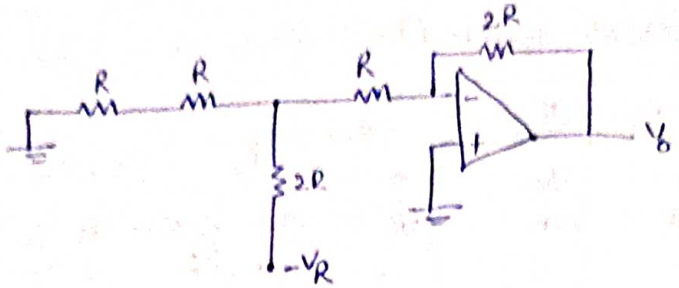
The equivalent circuit as



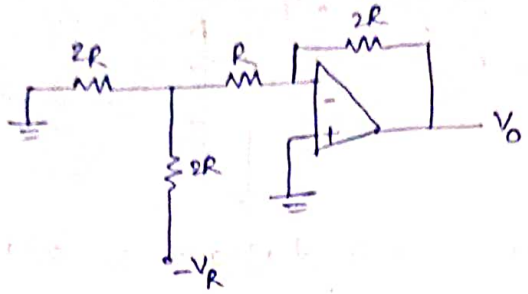
$$\frac{2R \times 2R}{2R+2R} = \frac{4R^2}{4R} = R$$







[∵ $\frac{2R \times 2R}{2R+2R} = \frac{4R^2}{4R} = R$]

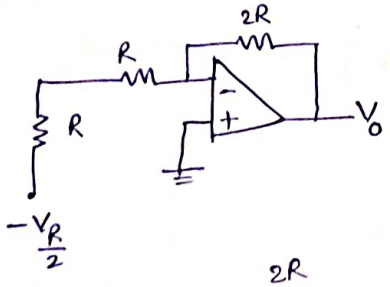


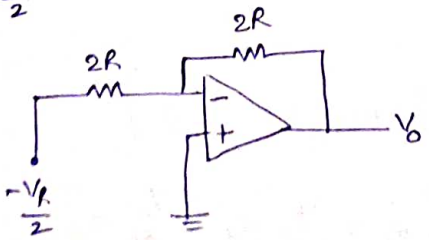
Apply Thevinin's voltage & Thevinin's resistance,

[∵ one resistance is connected to Ground & other one as -ve voltage so apply Thevinin theorem.]

$$V_{TH} = \frac{(-V_R)(2R)}{2R+2R} = \frac{-V_R \cdot 2R}{4R} = \frac{-V_R}{2}$$

$$R_{TH} = 2R \| 2R = R$$





The output voltage $V_0 = -\frac{2R}{2R} \cdot \left(\frac{-V_R}{2}\right)$

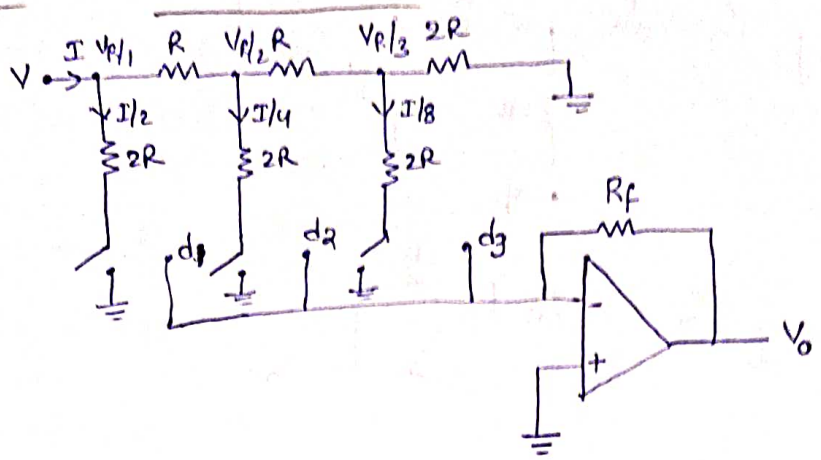
[∵ w.k.T Inverting op-Amp Gain $= -\frac{R_f}{R_1}$]

$$\boxed{V_0 = \frac{V_R}{2}}$$ → which is equivalent to binary Input 100

In general, output voltage is given by

$$\boxed{V_0 = -V_R (d_1 2^{-1} + d_2 2^{-2} + d_3 2^{3} + \text{-----} + d_n 2^{n})}$$

R-2R ladder DAC (current switched) :-



The main difference between circuit diagram in voltage switched & current switched as in place of OP-Amp we are connecting ground & In place of ground we are connecting OP-Amp.

$$I = \frac{V}{R}$$

Output voltage $V_0 = -I' R_f$

$$I' = \left[\frac{I}{2} + \frac{I}{4} + \frac{I}{8}\right] \quad \text{— FOR 3-bits}$$

FOR N-bits

$$I' = \left[\frac{I}{2} + \frac{I}{4} + \frac{I}{8} + ---- + \frac{I}{2^N}\right]$$

$$\Rightarrow V_0 = -R_f\left[\frac{I}{2} + \frac{I}{4} + \frac{I}{8} + -- + \frac{I}{2^N}\right]$$

$$= -R_f\left[\frac{V_R}{2R} d_1 + \frac{V_R}{4R} d_2 + \frac{V_R}{8R} d_3 + --- + \frac{V_R}{2^n R} d_n\right]$$

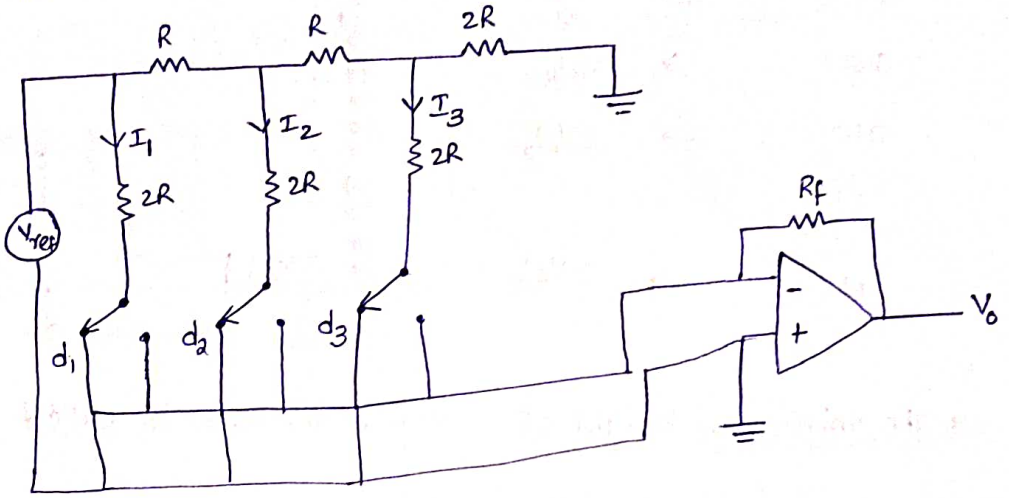
$$= -\frac{V_R R_f}{R}\left[d_1 2^{-1} + d_2 2^{-2} + ----- + d_n 2^{-n}\right]$$

If $R_f = R$,

$$\boxed{V_0 = -V_R\left[d_1 2^{-1} + d_2 2^{-2} + d_3 2^{-3} + ----- + d_n 2^{-n}\right]}$$

3. Inverted R-2R Ladder DAC :-

An Inverted R-2R Ladder type DAC employs voltage scaling, Identical resistors and Inverting summing OP-Amp.



$$I_1 = \frac{V_{ref}}{2R}$$

$$I_2 = \frac{\frac{V_{ref}}{2}}{2R} = \frac{V_{ref}}{4R}$$

$$I_3 = \frac{\frac{V_{ref}}{4}}{2R} = \frac{V_{ref}}{8R}$$

$\therefore$ The output voltage $V_o = -I_o R_f$

$$= -[I_1 + I_2 + I_3] R_f$$

$$= -R_f \left[\frac{V_{ref}}{2R} d_1 + \frac{V_{ref}}{4R} d_2 + \frac{V_{ref}}{8R} d_3 \right]$$

For N-bit,

$$V_o = -R_f \left[\frac{V_{ref}}{2R} d_1 + \frac{V_{ref}}{4R} d_2 + \frac{V_{ref}}{8R} d_3 + \cdots\cdots + \frac{V_{ref}}{2^n R} d_n \right]$$

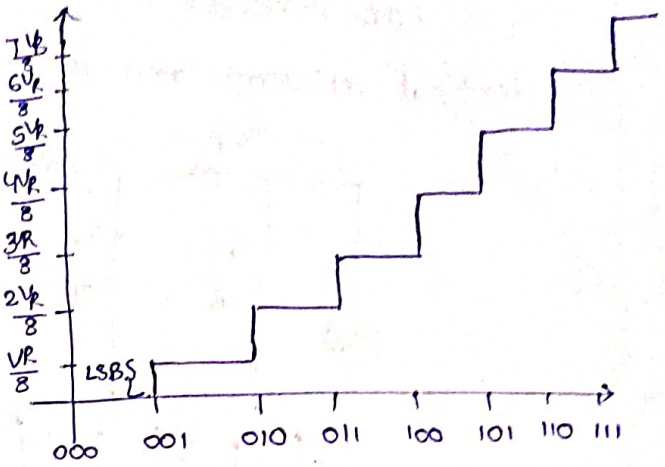
If $R_f = R$,

$$\boxed{V_o = -V_{ref} \left[\frac{d_1}{2} + \frac{d_2}{2} + \frac{d_3}{3} + \cdots\cdots + \frac{d_n}{2^n} \right]}$$

For 3-bit DAC,

$$V_0 = -V_{ref}\left[d_1 2^{-1} + d_2 2^{-2} + d_3 2^{-3}\right]$$

000	→	$\frac{V_0}{0}$
001	→	$V_R/8$
010	→	$2V_R/8$
⋮		
111	→	$7V_R/8$

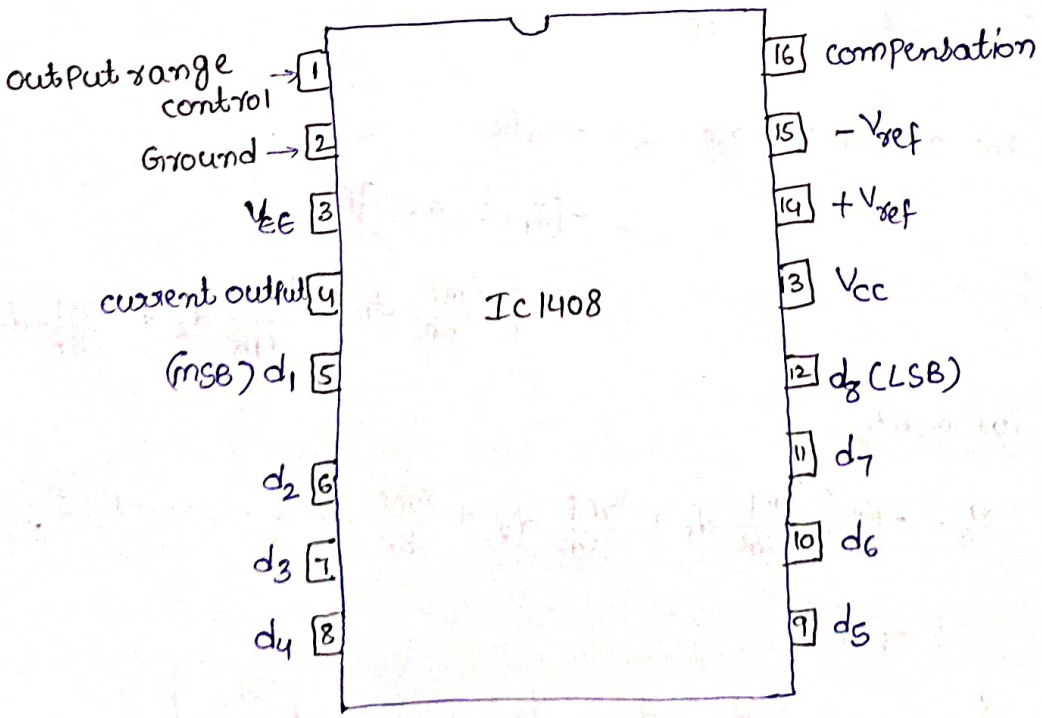


* The minimum height of each stair case is called Resolution (or) 1LSB

IC 1408 DAC :- (or) monolithic DAC :-

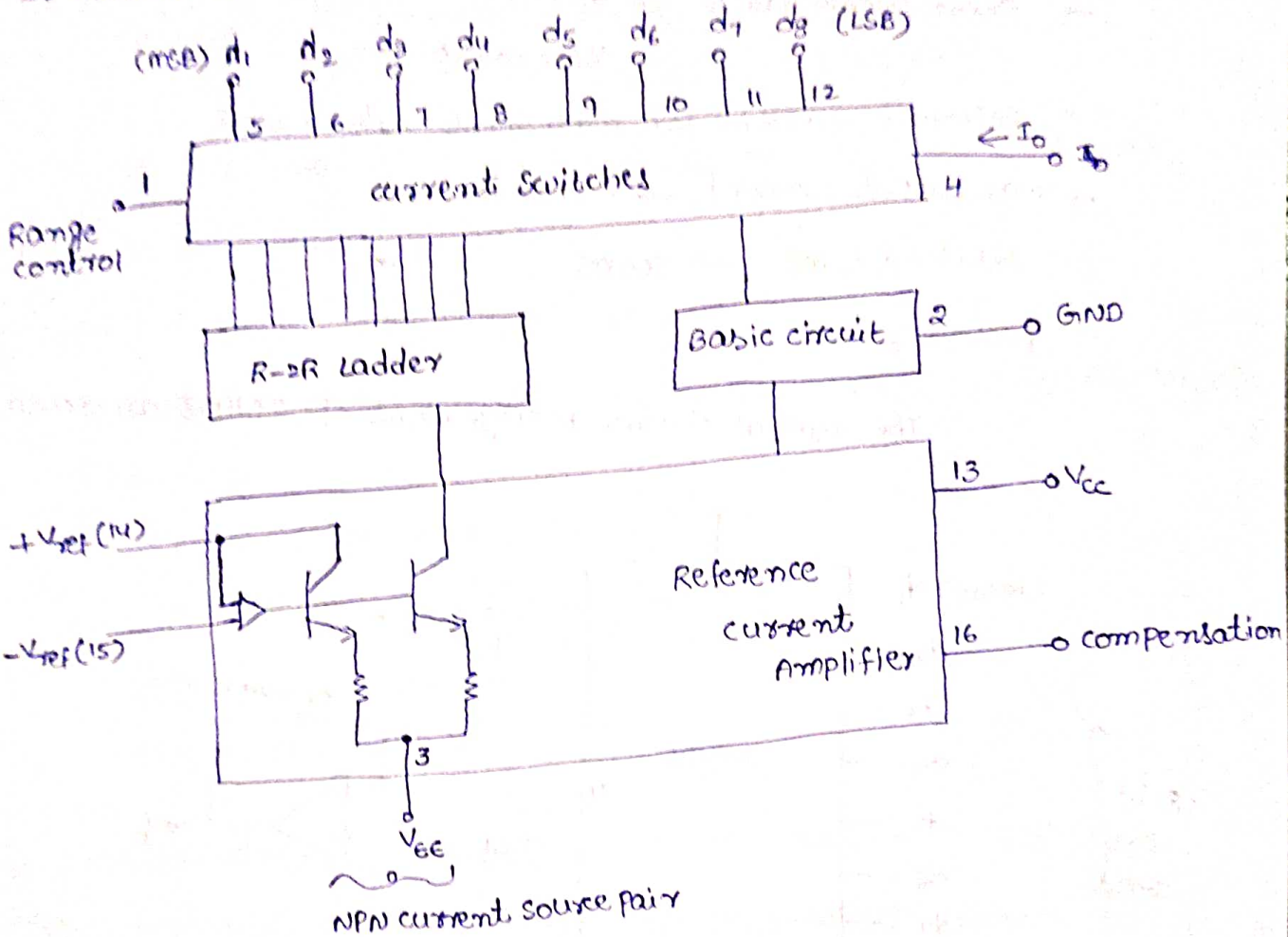
The Ic 1408 is an 8-bit R-2R Ladder type D/A converter.

The Pin configuration of Ic 1408 D/A Converter is shown in fig.



* The IC 1408 consists of an reference current Amplifier, R-2R ladder and 8-high speed current switches. It has 8-Input data lines d_1 (MSB) through d_8 (LSB).

* It consists of 2-power supplies $V_{CC} = 5V$, $V_{EE} = -15V$



The output current is given by

$$I_{out} = \frac{V_{ref}}{R_{14}} \left(\frac{d_1}{2} + \frac{d_2}{4} + \frac{d_3}{8} + \frac{d_4}{16} + \frac{d_5}{32} + \frac{d_6}{64} + \frac{d_7}{128} + \frac{d_8}{256} \right]$$

when all the data lines are at Logic high,

$$I_{out} = \frac{5}{2.5 \times 10^3} \left(\frac{1}{2} + \frac{1}{4} + \frac{1}{8} + \frac{1}{16} + \frac{1}{32} + \frac{1}{64} + \frac{1}{128} + \frac{1}{256} \right)$$

$$= 1.992 mA$$

The output current is converted into voltage by Itov converter.

The output voltage for full scale Input can be given as

$$V_o = 1.992 \times 10^{-3} \times 2.5 \times 10^3 = 4.98\,V$$

Characteristics of IC 1408 :-

→ power supply range → $V_{cc} = 5V$

$V_{ee} = -5V$ to $-15V$

→ Reference current for max. Input scale → 2mA

→ max. output current → 1.992mA

→ settling time → 300nS

→ Accuracy → 0.19%.

The typical circuit arrangement of IC1408 as shown in fig.

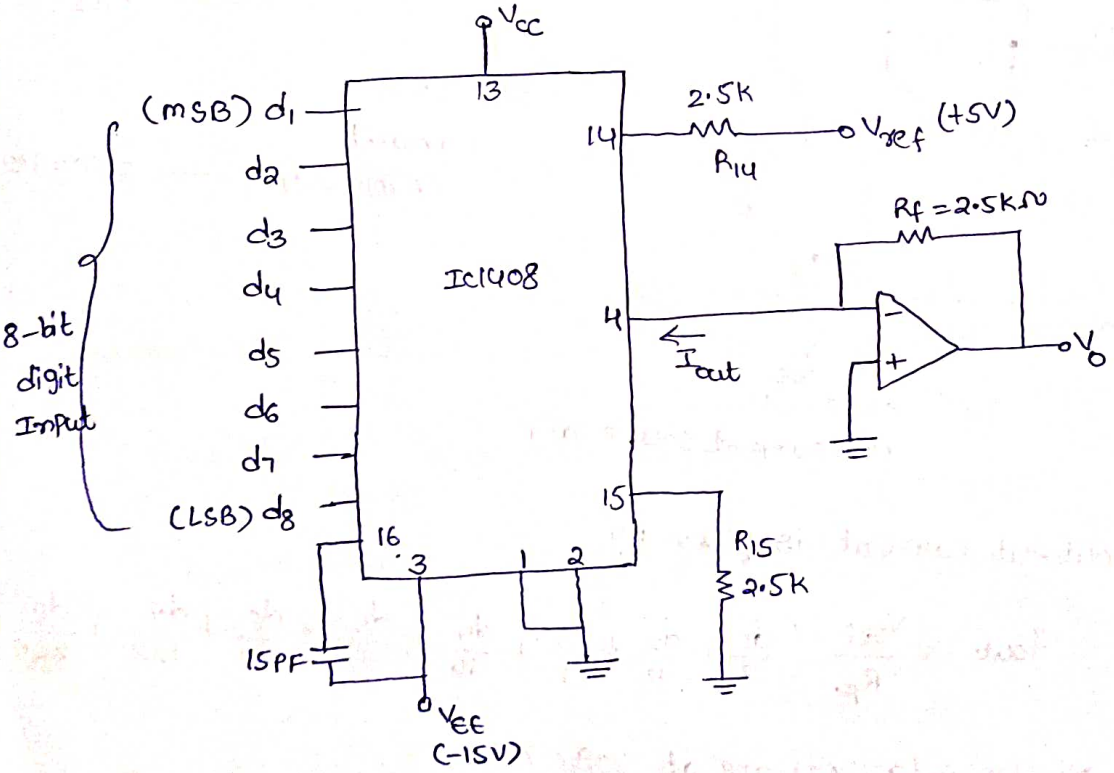
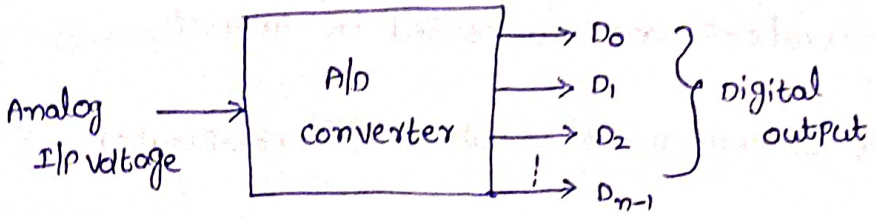


Fig :- Typical circuit of IC 1408

* From the figure, output in unipolar range.
* when digital Input is 00H, output voltage is 0V
* when digital Input is FFH, output voltage is 5V.

A/D converters :-



* The A/D conversion is a Quantizing process whereby an Analog signal is converted into equivalent binary word.

* There are 2 types based on the conversion techniques

i) comparing analog signal with Internally generated reference voltage

It contains

i) successive Approximation

ii) Flash (or) Parallel comparator type

iii) Delta modulated

iv) Adaptive delta modulated

ii) In this technique, changing an Analog signal into time (or) frequency and comparing these new parameters against known values.

It contains i) Integrator converters

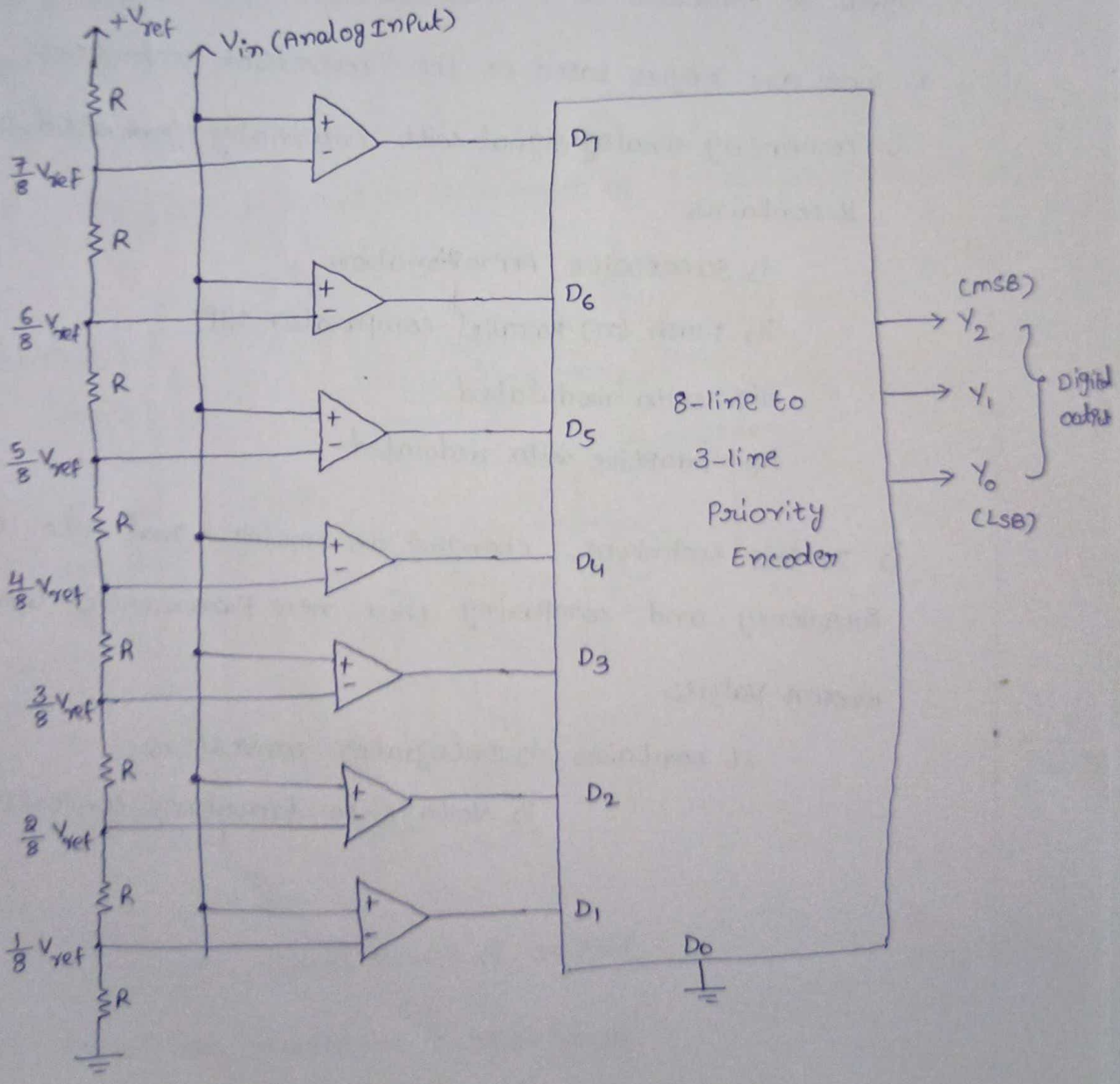
ii) voltage-to-frequency converters.

1. Parallel comparator type (or) Flash ADC :-

In this technique used to improve speed of operation, All the comparators are connected in parallel.

→ For n-bit conversion, it requires 2^{n-1} comparators & 2^n resistors

consider 3-bit flash A/D converter, it contains $2^{3-1} = 2^3 - 1 = 7$ comparators (or) op-Amps and 2^3 resistors.



* From the figure, one Input of each comparator is connected to Input signal and other Input to reference voltage.

* The comparator give output 1 (or) 0 it depending on Input signal and reference signal.

If $V_{in} > V_{ref}$ → The output of comparator is High (1)

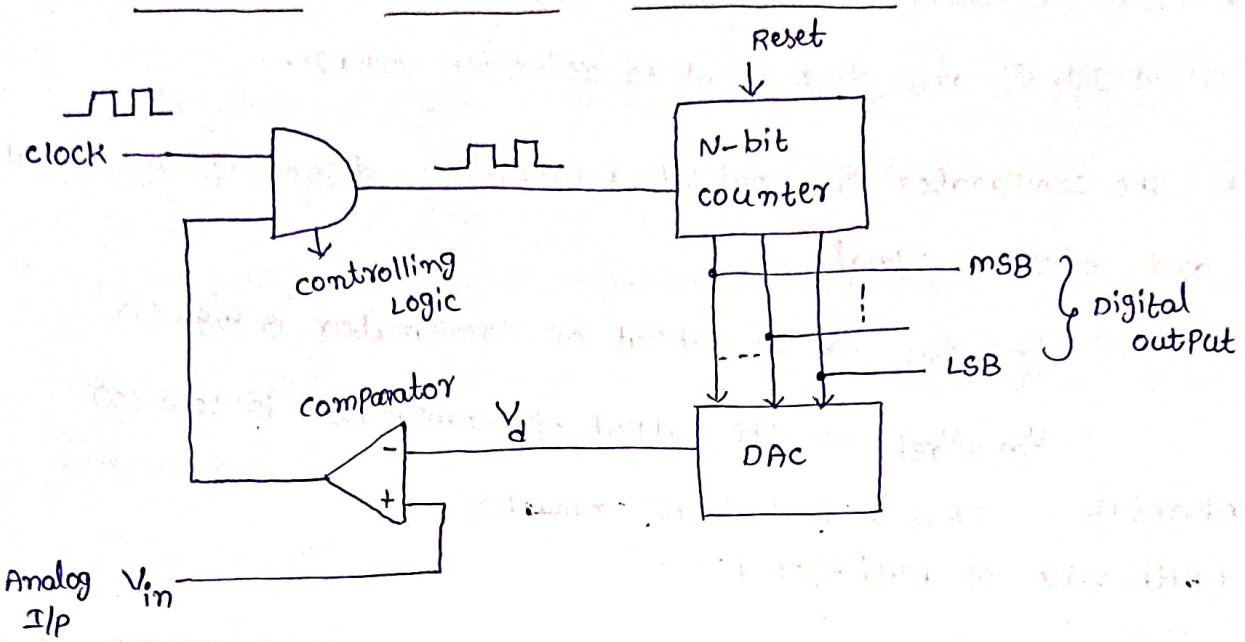
$V_{in} < V_{ref}$ → The output of comparator is Low (0)

Advantage → It is a fastest A/D converter

Truth table of Flash type ADC :-

Input voltage	comparator outputs								Digital output		
	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Y_2	Y_1	Y_0
$0 < V_{in} < \frac{V_{ref}}{8}$	0	0	0	0	0	0	0	1	0	0	0
$\frac{V_{ref}}{8} < V_{in} < \frac{2V_{ref}}{8}$	0	0	0	0	0	0	1	x	0	0	1
$\frac{2V_{ref}}{8} < V_{in} < \frac{3V_{ref}}{8}$	0	0	0	0	0	1	1	x	0	1	0
$\frac{3V_{ref}}{8} < V_{in} < \frac{4V_{ref}}{8}$	0	0	0	0	1	1	1	x	0	1	1
$\frac{4V_{ref}}{8} < V_{in} < \frac{5V_{ref}}{8}$	0	0	0	1	1	1	1	x	1	0	0
$\frac{5V_{ref}}{8} < V_{in} < \frac{6V_{ref}}{8}$	0	0	1	1	1	1	1	x	1	0	1
$\frac{6V_{ref}}{8} < V_{in} < \frac{7V_{ref}}{8}$	0	1	1	1	1	1	1	x	1	1	0
$V_{in} > \frac{7V_{ref}}{8}$	1	1	1	1	1	1	1	x	1	1	1

2. counter type (or) Ramp type A/D converter :-



* In this type, the output of DAC is continuously compared with Analog Input to ADC which is to be converted into digital output.

Operation:-

i) Initially, the counter is Reset, i.e output is zero by applying a reset pulse. The output of counter is given to Input of DAC it Produces as zero i.e $V_d = 0$.

ii) when $V_{in} > V_d$, the output of comparator becomes high.

iii) It is given to 1 Input of AND gate, and 2nd Input is clock Pulses.

i.e For an AND gate, one input is clock Pulses and other input is output of comparator. Because of high output of comparator, the clock Pulses are allowed to pass through AND gate.

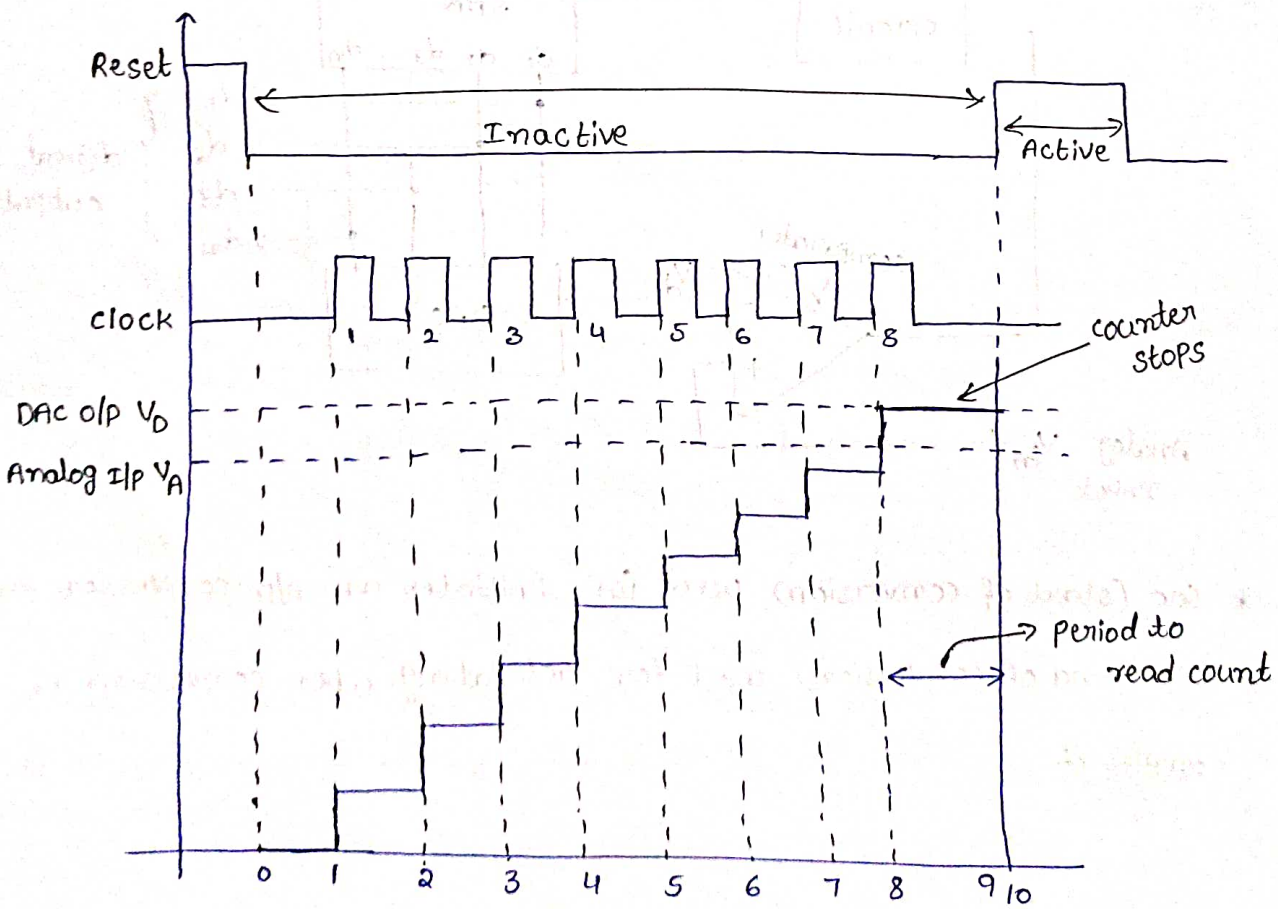
iv) The counter starts counting these clock pulses. According to No. of clock pulses, the output of counter Increasing. It Increases output of DAC.

v) If $V_{in} < V_d$, the output of comparator becomes Low.

This disables AND gate, so the clock pulses are not allowed to pass through AND gate. The counting process of N-bit counter is stopped.

→ In this type, we are using $2^N - 1$ clock pulses.

Waveforms:-



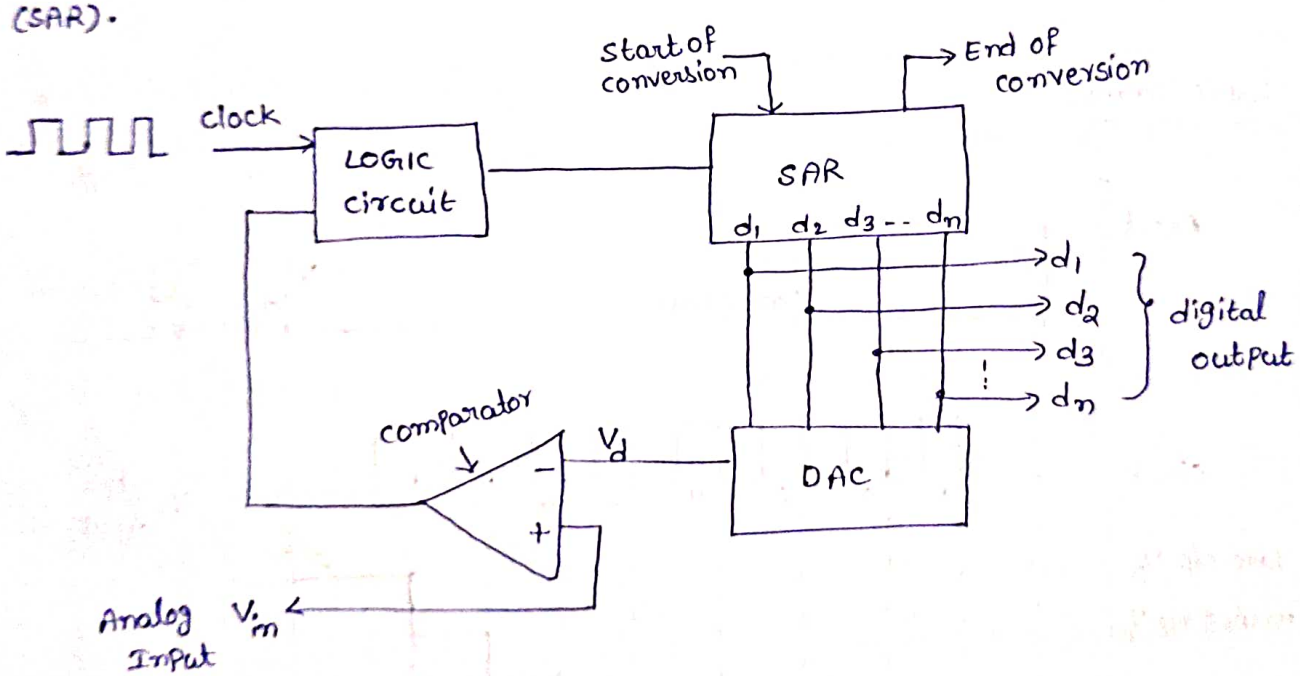
Disadvantages:-

→ There is a limitation in clock frequency, As clock frequency is Low, speed of conversion is less.

→ conversion time is not constant. It Increases with Increase in Input voltage. (or) conversion time is high at high Input voltage.

3. Successive Approximation type A/D converter :-

It consists of DAC, comparator, successive approximation register (SAR).



* Soc (Start of conversion) used for Initiates an A/D conversion Process.
* Eoc (End of conversion) used for activating when conversion is completed.

The SAR consists of 2 conditions

i) when ever switch is ON, MSB of SAR set to '1'.

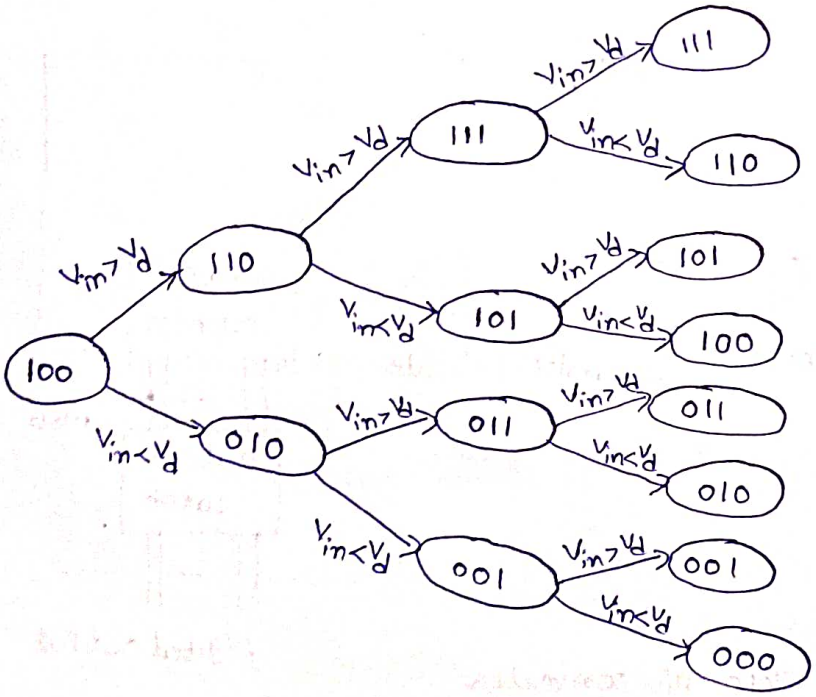
ii) when $V_{in} > V_d$ → set your next bit (from MSB to LSB)

when $V_{in} < V_d$ → Already set bit is going to reset and it will set next bit.

For example, consider $V_{in}=3$ (3-bit sucessive Approximation)

The Input is 3-bits,

i) switch is ON, MSB set to '1' i.e 100 (3-bits)



* In this case we are using 3-bits so, 3-clock cycles are used

* For N-bit, we can use N-clock cycles.

* The time for one Analog to digital conversion must depend on both the clock's period T and No. of bits 'n'.

It is given as,

$$T_c = T(n+1)$$

where $T_c \rightarrow$ conversion time

$T \rightarrow$ clock period

$n \rightarrow$ No. of bits

4. Dual-Slope ADC :-

Dual slope conversion is an Indirect method for A/D conversion where an Analog voltage & reference voltage are converted into Timeperiods by an Integrator & measured by counter.

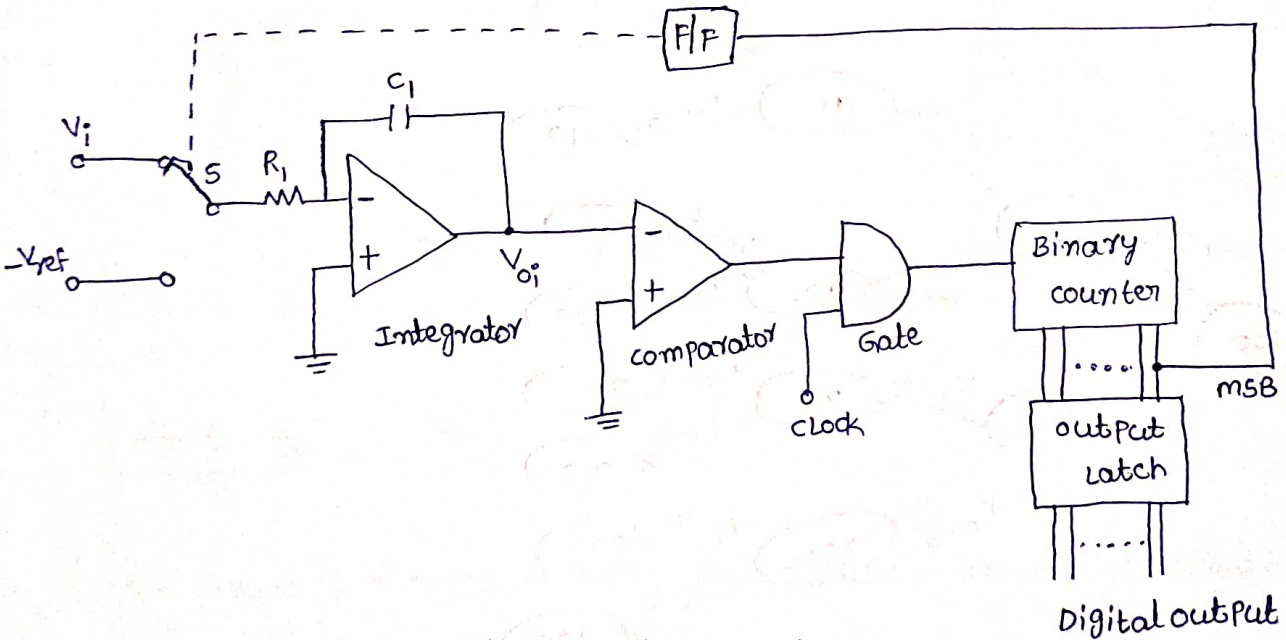


Fig :- Dual Slope A/D converter

* It consists of Integrator (Ramp generator), comparator, Binary counter, output latch and reference voltage.

→ Integrator Input is switched between Analog Input voltage V_i and negative reference voltage, $-V_{REF}$.

→ Analog switch is controlled by MSB of counter.

when MSB = Logic 0 → Analog Input is connected to Integrator

when MSB = Logic 1 → -Ve Reference Voltage is connected to ramp -generator (Integrator)

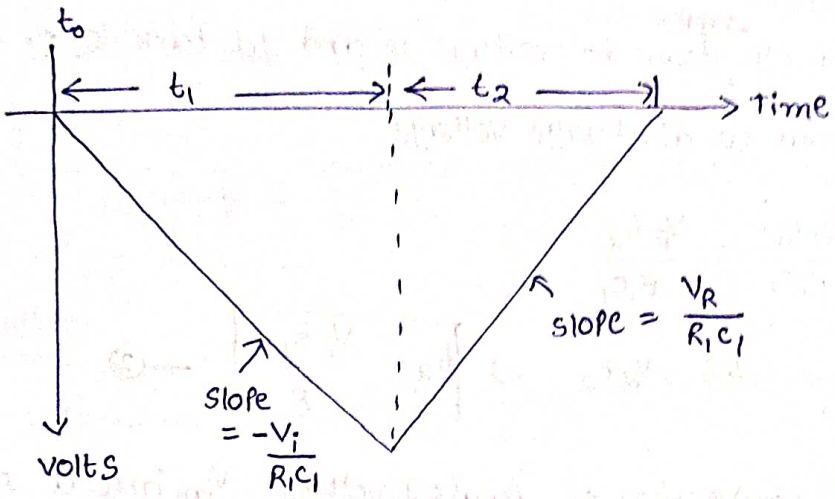


Fig :- Integrator output voltage

At time $t=0$, Analog switch 'S' is connected to Analog Input voltage V_i, so that Analog Input voltage Integration begins.

The output voltage is

$$V_{oi} = \frac{-1}{R_1C_1}\int_0^t V_i\,dt$$

$$= \frac{-V_i t}{R_1C_1} \quad \text{—①}$$

$R_1C_1 \rightarrow$ Time const.

$V_i \rightarrow$ also constant.

→ At the end of 2^N clock periods MSB of counter goes high. It gives flip flop also high, which causes analog switch 'S' to be switched from V_i to $-V_R$.

→ The -ve Input voltage ($-V_R$) connected to Input of Integrator causes the Integrator output to ramp positive.

→ When Integrator output reaches to zero, comparator output voltage goes low, which disables clock AND gate. This stops clock pulses reaches the counter, so that counter will be stopped at a count corresponding to No. of clock Pulses in time t_2.

→ Integrator o/p ramp down to voltage V and get back to 0. so, charge voltage is equal to discharge voltage,

$$\frac{V_i t_1}{R_1 C_1} = \frac{V_R t_2}{R_1 C_1}$$

$$V_i t_1 = V_R t_2 \Rightarrow \boxed{t_2 = \frac{V_i t_1}{V_R}} \quad -(2)$$

→ The actual conversion of Analog voltage V_{in} into a digital count occurs during t_2.

The control circuit connects the clock to counter at begining of t_2. The clock is disconnected at end of t_2. Thus counter contains digital output

$$\therefore \text{Digital output} = \left(\frac{\text{counts}}{\text{second}}\right) t_2 \quad -(3)$$

From eq(2)

$$\text{Digital output} = \left(\frac{\text{counts}}{\text{seconds}}\right) t_1 \left(\frac{V_i}{V_R}\right) \quad -(4)$$

The counter o/p is connected to digital display.

Advantages

→ High accurate
→ Low cost
→ Immune to temperature caused variations in R_1, C_1.

Disadvantage

* Low speed

Performance Specifications of DAC :-

1. Accuracy:-

It is defined as the difference between measured output and actual output.

→ Absolute accuracy refers to maximum deviation of measured output from the actual output value.

→ It is expressed in percentage of its full scale voltage (or) fractions of $\pm\frac{1}{2}$ of its LSB.

$$\text{Accuracy} = \frac{V_{OFS}}{(2^n-1)2}$$

2. Resolution:-

→ It is defined as no. of different analog output values provided by a DAC.

For n-bit DAC → Resolution $= 2^n$

→ It also stated that, the ratio of change in output voltage resulting from a change of 1 LSB at digital inputs.

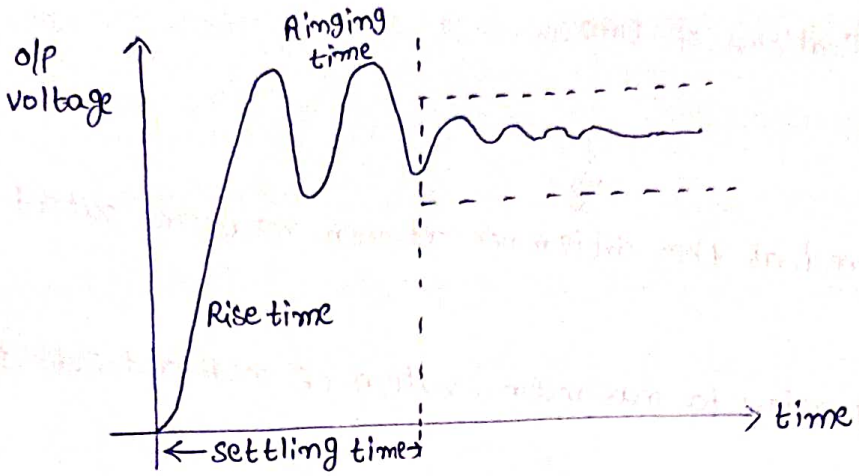
For n-bit DAC → $\text{Resolution} = \frac{V_{OFS}}{2^n-1}$

where, V_{OFS} → Full scale output voltage.

3. Settling time :- (Conversion time)

It is defined as the time taken by the output of converter to reach and stay with in $\pm\frac{1}{2}$ LSB of its final value for a given change in input.

→ Settling time of a converter varies between 100ns to 10μs.



4. Dynamic range:-

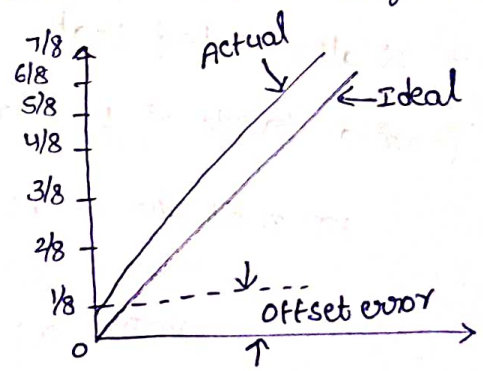
It is defined as the ratio of largest output to the smallest output, excluding zero.

→ It is expressed in dB.

Dynamic range = $20 \log 2^n \approx 6n$.

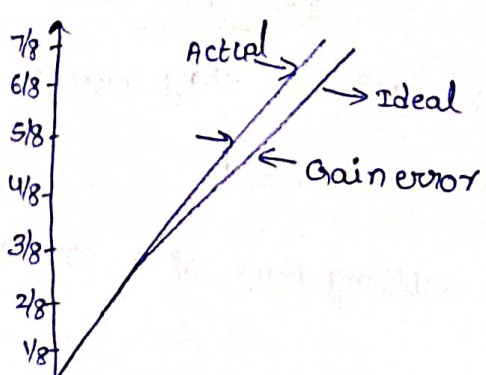
5. offset error:-

It is defined as the nonzero level of output voltage when all inputs are zero.



6. Gain error:-

It is defined as the difference between the caluclated gain of the current to voltage converter & actual gain achieved.



7. Stability :-

The performance of converter changes with temperature, age and power supply variations. So all the parameters such as offset, gain, linearity error and monotonicity must be specified over the full temperature and power supply ranges.

These parameters represent the stability of converter.

8. monotonicity:-

It is defined as No variations (or) linear Increase in Analog output for an Increase in digital Input.

→ If the output of DAC does not Increases linearly (or) some times decreases for linear Increase in Input, then DAC is said to be Non-monotonic DAC.

9. Linearity :-

The term linearity describes how close the measured output appears to Its Ideal (actual) transfer characteristics. Thus, linearity of a DAC is defined as a measure of its accuracy.

→ In case of Ideal DAC, the o/p linearly Increases for an Increase in Input.

→ In case of Practical, the o/p is not linear even though there is an Equal Increment in output.

Performance Specifications of ADC :-

1. Resolution:-

i) Same as DAC definition

ii) It also defined as, the ratio of change in Input voltage resulting from a change of 1LSB at digital outputs.

For n-bit ADC, Resolution $= \frac{V_{iFS}}{2^n - 1}$

where, V_{iFS} → Full scale Input voltage.

2. conversion time (or) settling time :-

It is defined as the total time required to convert an Analog siginal into to digital output.

→ It depends on conversion technique ~~based~~ used and the propagation delay of circuit parameters.

AD574A (12-bit A/D converter) specifications :-

It requires no external components to provide the complete successive approximation based on Analog to digital conversion. The performance specifications are given as

1. Power supply
   - i) Positive power supply voltage V_{CC} : +11.4 to +16.5
   - ii) negative power supply voltage V_{EE} : -11.4 to -16.5
   - iii) V_{Logic} : +4.5 to +5.6
2. Resolution : 12-bit
3. Linearity error : ±1LSB
4. Temperature range : 0 to 70°C
5. Analog Input range : -5 to +5V
6. Internal reference voltage : 9.98 to 10.02
7. maximum conversion time : 35 µS
8. operating current
   - I_{LOGIC} : 30-40mA
   - I_{CC} : 2-5 mA
   - I_{EE} : 18-30mA
9. Power dissipation : 390 mw (Typical)
   : 725 mw (maximum)

Problems

1. The LSB of a 10-bit DAC is 20mV

i) what is % resolution ii) what is full scale range

iii) what is o/p voltage for an input, 10110 01101

Sol:-

i) % resolution $= 20\times10^{-3}\times100 = 2\%$

ii) $V_{FS} = 2^n - 1 \times \text{Resolution} = 2^{10} - 1 \times 0.2 = 20.46$

iii) $(1011001101)_2 = (1\times2^9 + 0\times2^8 + 1\times2^7 + 1\times2^6 + 0\times2^5 + 0\times2^4 + 1\times2^3 + 1\times2^2 + 0\times2^1 + 1\times2^0)$

$= 512 + 128 + 64 + 8 + 4 + 1 = 717$

$\therefore$ output voltage $V_{out} = 717\times20\times10^{-3} = 14.34\,V$

---

2. LSB of 9-bit DAC is represented by 19.6mV. If an input of 9 zero bits is represented by 0V.

i) Find the out put of DAC for an Input, 10110 1101 and 01101 1011

ii) what is the Full scale reading (FSR) of this DAC.

Sol:-

i) $(101101101)_2 = 1\times2^8 + 0\times2^7 + 1\times2^6 + 1\times2^5 + 0\times2^4 + 1\times2^3 + 1\times2^2 + 0\times2^1 + 1\times2^0$

$= 365$

output $V_{out} = 365\times19.6\times10^{-3} = 7.15\,V$

ii) $(011011011)_2 = 0\times2^8 + 1\times2^7 + 1\times2^6 + 0\times2^5 + 1\times2^4 + 1\times2^3 + 0\times2^2 + 1\times2^1 + 1\times2^0$

$= 219$

$\therefore V_{out} = 219\times19.6\times10^{-3} = 4.29\,V$

ii) Full scale reading (FSR) $= (2^n - 1)$ of 19.6mV

$= (2^9 - 1)\times19.6\times10^{-3}$

$= 10$ Volts

---

3. calculate the conversion time for a full scale input in case of 12-bit counter type Analog to digital converter driven by 2MHz clock.

Sol: $T = \frac{1}{2\times10^6} = 0.5\mu s$

For 12-bit counter type $= (2^n - 1) \times T$

$= (2^{12} - 1) \times 0.5 \times 10^{-6} = 2.047\ ms$

4. If the max. output voltage of 7bit DAC is 25.4 V, what is the Smallest change in output as the binary count Increases.

Sol: $\text{Resolution} = \frac{V_{FS}}{2^n - 1} = \frac{25.4}{2^7 - 1} = 0.2V$

5. Determine o/p voltage produced by a 4bit DAC whose o/p voltage range is 0 to 10V when the binary no. is 0110

Sol: G.T $V_{FS} = 10V$

$\text{Resolution} = \frac{10}{2^4 - 1} = 0.6667\ V$

o/p voltage at 0110 $= 0.6667 \times 6 = 4V$

6. Determine the resolution of an 8-bit ADA ADC for an 10V Input.

Sol: $\text{Resolution} = \frac{V_{FS}}{2^n - 1} = \frac{10}{2^8 - 1} = 39.215\ mV$

7. calculate the no. of bits required to represent a full scale voltage of 10V with a resolution of 5mV approximately.

Sol: $\text{Resolution} = \frac{V_{FS}}{2^n - 1} \Rightarrow 2^n - 1 = \frac{V_{FS}}{\text{Resolution}}$

$\Rightarrow 2^n = \frac{V_{FS}}{\text{Resolution}} + 1 = \frac{10}{5\times10^{-3}} + 1 = 2001$

$\Rightarrow 2^n = 2001$

when $n = 11$, we have $2^n = 2048$, $\therefore$ minimum 11 bits are required to represent a full scale voltage of 10V.

8) A 12-bit D to A converter has a full scale range of 15V. Its max. differential linearity error is $\pm \frac{1}{2}$ LSB.

i) what is the Percentage resolution

ii) what are min. and max. possible values of Increment in its output voltage.

Sol- G.T $n=12$, $V_{OFS} = 15V$

i) Percentage resolution :-

$$\% \text{ Resolution} = \frac{V_{OFS}}{2^n - 1} \times 100 = \frac{15}{2^{12}-1} \times 100$$

$$= 0.366\% \text{ Volts}$$

ii) min. and max. values of output voltage :-

$$MSB = \frac{V_{OFS}}{2} = \frac{15}{2} = 7.5V$$

$$LSB = \frac{V_{OFS}}{2^n} = \frac{15}{2^{12}} = 3.66mV$$

---

9) An Inverted R-2R Ladder type digital to Analog converter $R=10K\Omega$, $V_{ref} = +20V$ find the current in each $20K\Omega$ resistor and max. current Passing into feed back resistor OP-AMP.

Sol- G.T $R=10K\Omega$, $V_{ref} = 20V$, $2R=20K\Omega$

Let Inverted R-2R Ladder type D/A converter is 4-bit converter

i.e $n=4$

$$I_1 = \frac{V_{ref}}{2R} = \frac{20}{2\times10^3} = 1mA$$

$$I_2 = \frac{V_{ref}/2}{2R} = \frac{V_{ref}/2R}{2} = \frac{I_1}{2} = \frac{1mA}{2} = 0.5mA$$

$$I_3 = \frac{V_{ref}/4}{2R} = \frac{V_{ref}/4R}{2} = \frac{I_2}{2} = \frac{0.5mA}{2} = 0.25mA$$

$$I_4 = \frac{V_{ref}/8}{2R} = \frac{V_{ref}/8R}{2} = \frac{I_3}{2} = \frac{0.25}{2} = 0.125mA$$

The output voltage of D/A converter is given by

$$V_{out} = -I_{out} R_f$$

$$= -[I_1 + I_2 + I_3 + I_4] R \qquad [\because R_f = R]$$

$$= -\left[\frac{V_{ref}}{2R} + \frac{V_{ref}}{4R} + \frac{V_{ref}}{8R} + \frac{V_{ref}}{16R}\right] R$$

$$= -V_{ref}\left[\frac{1}{2} + \frac{1}{4} + \frac{1}{8} + \frac{1}{16}\right]$$

$$= -20\left[\frac{1}{2} + \frac{1}{4} + \frac{1}{8} + \frac{1}{16}\right] = -18.75\,V$$

10) Design a 4-bit weighted resistor DAC whose full-scale output voltage is -5V. Assume $R_f = 10k\Omega$, Logic '1' level as +5V, Logic '0' level as '0' volts. What is the output voltage when Input is 1011.

Sol:- G.T $V_{OFS} = -10V$, $R_f = 10k\Omega$, Logic '1' level as +5V
Logic '0' level as 0V

The output voltage is, $V_{out} = I_{out} R_f$

$$= \frac{V_R}{R} R_f \left[\frac{d_1}{2} + \frac{d_2}{2^2} + \frac{d_3}{2^3} + \frac{d_4}{2^4}\right]$$

If $R_f = R$, $V_R = V_{OFS} = -10V$ then

$$\therefore V_{out} = -10\left[5 \times 2^{-1} + 0 \times 2^{-2} + 5 \times 2^{-3} + 5 \times 2^{-4}\right]$$

$$= -10[3.4375]$$

$$\therefore V_{out} = -34.375\,V$$

[$\because$ '1' → 5 & '0' → as '0'
Input → 1011
5 0 5 5].