Code No: R1931043 **R19** **SET - 1**

III B. Tech I Semester Supplementary Examinations, June/July-2022

DIGITAL COMMUNICATIONS

(Electronics and Communication Engineering)

Time: 3 hours Max. Marks: 75

Answer any **FIVE** Questions **ONE** Question from **Each unit**
All Questions Carry Equal Marks
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UNIT-I

1. a) Explain how the compressor and expander are used for non-uniform quantization. [8M]
   b) Explain why delta modulation is a special case of DPCM. [7M]

(OR)

2. a) What do you understand by aperture effect? Explain. [8M]
   b) For a PCM signal, find $L = 2^n$ if the compression parameter $\mu = 100$ and the minimum required SNR is 40 dB. Determine the output SQNR. [7M]

UNIT-II

3. a) Explain the decoding logic for DPSK demodulator. [8M]
   b) What are the different signaling techniques? Explain. [7M]

(OR)

4. a) What are the different schemes that are used for digital data transmission? Explain briefly. [8M]
   b) In wireless digital communication, it is observed that as the received signal strength reduces, the rate of data transfer also reduces. Explain the reason by means of constellation diagram. [7M]

UNIT-III

5. a) Draw the block diagram of coherent ASK receiver, and explain its operation with necessary equations. [8M]
   b) Explain why the matched filter is called as an optimum filter. [7M]

(OR)

6. a) Explain how the Schwartz inequality is used to find $H_{opt}(f)$ of a matched filter. [8M]
   b) Explain how the FSK signal is demodulated using coherent receiver. [7M]

UNIT-IV

7. a) A discrete memoryless source has symbols A, B and C as its alphabet with corresponding probabilities 0.5, 0.3 and 0.2 respectively. Compute the entropy of the source and develop the code using Huffman source coding algorithm. [8M]
   b) Define mutual information and list its properties. [7M]

Code No: R1631044 **R16** **SET - 1**

III B. Tech I Semester Supplementary Examinations, June/July-2022

DIGITAL COMMUNICATIONS

(Electronics and Communication Engineering)

Time: 3 hours Max. Marks: 70

Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B)**
2. Answer **ALL** the question in **Part-A**
3. Answer any **FOUR** Questions from **Part-B**

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PART –A (14 Marks)

1. a) Explain the importance of prediction in DPCM. [2M]
   b) Write the different types of digital modulation techniques. [2M]
   c) Compare a correlator and a matched filter. [2M]
   d) What is average information? What is its significance? [3M]
   e) For a noiseless channel with 'm' input symbols and 'm' output symbols, prove that H(X) =H(Y). [3M]
   f) Compare linear block codes and cyclic codes. [2M]

PART –B (56 Marks)

2. a) Explain the delta modulation in detail with suitable diagrams. [7M]
   b) Draw the block diagram of adaptive delta modulation and explain its operation. [7M]

3. a) Determine the bandwidth required for M-ary FSK system. Draw the geometrical representation of M-ary FSK signals and find out the distance between the signals. [7M]
   b) Draw the block diagram of M-ary PSK system and explain its operation. [7M]

4. Explain about coherent binary PSK transmitter and receiver. Assuming channel noise to be additive white Gaussian obtain expression for probability of error. [14M]

5. a) Explain the concept of amount of information and its properties. [7M]
   b) A discrete source emits one of five symbols once every 2 milliseconds. The symbol probabilities are: 1/2, 1/4, 1/8, 1/16 and 1/16 respectively. Find the source entropy and information rate. [7M]
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Code No: R1631045 **R16** **SET - 1**

III B. Tech I Semester Supplementary Examinations, June/July-2022

ANTENNA AND WAVE PROPAGATION

(Electronics and Communication Engineering)

Time: 3 hours Max. Marks: 70

Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B)**
2. Answer **ALL** the question in **Part-A**
3. Answer any **FOUR** Questions from **Part-B**

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PART –A (14 Marks)

1.	a)	Define half power beamwidth of antenna.	[2M]
	b)	Write the applications of loop antenna.	[2M]
	c)	Define first side lobe ratio.	[2M]
	d)	List out the some applications of helical antenna.	[3M]
	e)	Write the applications of Horn antennas.	[3M]
	f)	What is Duct Propagation?	[2M]

PART –B (56 Marks)

2.	a)	Discuss the following: (i) Normalized field pattern (ii) Main lobes and side lobes (iii) Directivity	[7M]
	b)	Explain the concept of antenna apertures in detail.	[7M]
3.	a)	Discuss about radiation from quarter wave monopole.	[7M]
	b)	Explain about radiation resistance of loop antenna.	[7M]
4.	a)	Write the salient features of uniform linear array.	[7M]
	b)	Explain the basic principles of ordinary end fire array.	[7M]
5.	a)	Write the salient features of microstrip antennas.	[7M]
	b)	Discuss the working principle of V-antenna.	[7M]
6.	a)	What is parabolic reflector? Explain its operating principles.	[7M]
	b)	Write the procedure for directivity measurement of antenna?	[7M]
7.	a)	What is ground wave? Explain the basics of wave propagation using ground wave.	[7M]
	b)	Explain how the space wave filed strength is influenced by curvature of earth and roughness of earth.	[7M]

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Code No: R193104A **R19** **SET - 1**

III B. Tech I Semester Supplementary Examinations, June/July-2022

INFORMATION THEORY & CODING

(Electronics and Communication Engineering)

Time: 3 hours Max. Marks: 75

Answer any **FIVE** Questions **ONE** Question from **Each unit**
All Questions Carry Equal Marks
*****

UNIT-I

1 a) Define coding efficiency. Derive the relation between coding efficiency and entropy. [8M]

b) A source emits independent sequence of symbols from an alphabet consisting of five symbols from an alphabet with probabilities 1/4, 1/8, 1/8, 3/16, 5/16 respectively. Find the Shannon code using Shannon encoding algorithm and compute the efficiency. [7M]

(OR)

2 a) What is information? Show that amount of information is equal to $-\log p(x_j)$? [8M]

b) A source produces six message with probabilities 1/4, 1/4, 1/8, 1/8, 1/8, 1/8. Obtain the information content of each message and the entropy. [7M]

UNIT-II

3 a) Derive the relation between mutual information and entropy. [8M]

b) A Gaussian channel has bandwidth of 1MHz. [7M]

(i) Calculate the channel capacity if the signal power to noise spectral density ratio is 10^5 Hz.

(ii) Find the maximum information rate.

(OR)

4 a) Prove I(X;Y) = I(Y;X). [8M]

b) What is channel capacity and channel efficiency? Define redundancy. [7M]

UNIT-III

5. a) For a systematic (6, 3) linear block code, the parity matrix 'P' is given by P = [8M]

$$\begin{bmatrix} 1 & 0 & 1 \\ 0 & 1 & 1 \\ 1 & 1 & 0 \end{bmatrix}$$

(i) Construct table for code words.

(ii) If the received bit pattern R = [1 0 1 1 0 0], determine the syndrome, correctable error pattern and corrected code vector for a single bit error.

Code No: R193104B **R19** **SET - 1**

III B. Tech I Semester Supplementary Examinations, June/July-2022

DIGITAL SYSTEM DESIGN USING HDL

(Electronics and Communication Engineering)

Time: 3 hours Max. Marks: 75

Answer any **FIVE** Questions **ONE** Question from **Each unit**
All Questions Carry Equal Marks
*****

UNIT-I

1. a) Write down the step by step approach of FPGA design process on XILINX environment. [8M]
   b) Draw and explain the basic architecture of FPGA. [7M]

(OR)

2. a) With the help of example explain the structure of a Verilog test bench file. [8M]
   b) Explain three different methods of modeling in describing a digital system in Verilog with examples. [7M]

UNIT-II

3. a) Give the syntax for a net declaration? Explain the different kind of nets that belong to the net data type. [8M]
   b) What are the different arithmetic operators in Verilog? Write a Verilog code for arithmetic operations on two eight bit vectors. [7M]

(OR)

4. a) List out the five different kinds of variable data types. Explain each one with declaration. [8M]
   b) Construct a primitive calculator to add, subtract, multiply and divide two 4-bit numbers on the Basys3 board in Verilog. [7M]

UNIT-III

5. a) Distinguish between combinational and sequential circuits. List some applications of sequential circuits. [8M]
   b) Implement the Verilog HDL source code and logic diagram for 1-bit full adder using data flow style. [7M]

(OR)

6. a) Draw the schematic circuit of a D flip flop with negative edge triggering using NAND gates. Give its truth table and explain its operation. [8M]
   b) Explain the modeling approach for static RAM memory using Verilog HDL. Modeling approach consists of design and implementation. [7M]

Code No: R1931044 **R19** **SET - 1**

III B. Tech I Semester Supplementary Examinations, June/July-2022

ELECTRONIC MEASUREMENTS & INSTRUMENTATION

(Electronics and Communication Engineering)

Time: 3 hours Max. Marks: 75

Answer any **FIVE** Questions **ONE** Question from **Each unit**

All Questions Carry Equal Marks

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UNIT-I

1. a) Explain in detail the different types of errors in measuring instruments. [8M]
   b) Explain with neat circuit diagram the working of any one type of digital voltmeter. [7M]

(OR)

2. a) A basic D'Arsonval movement with a full deflection of 50 μA and internal resistance of 500 Ω is used as voltmeter. Formulate the necessary equation and calculate the value of multiplier resistance needed to measure a voltage range of 0-10 V. [8M]
   b) How is multi-meter used to measure different parameters? Explain. [7M]

UNIT-II

3. a) Draw the block diagram of an audio spectrum analyzer. Explain its operation. [8M]
   b) Define a Wave Analyzer and list its types. [7M]

(OR)

4. a) With neat sketch explain the working principle of function generator. [8M]
   b) What are the different Types of Harmonic Distortion? Define Total Harmonic Distortion (THD). [7M]

UNIT-III

5. a) Explain the internal structure of CRT and describe the principle of electrostatic focusing. [8M]
   b) Compare analog storage oscilloscope and digital storage oscilloscope. [7M]

(OR)

6. a) Explain the modes of operation of digital storage oscilloscope. [8M]
   b) Describe the different types of sweeps used in CRO. [7M]

UNIT-IV

7. a) Describe the circuit of Kelvin double bridge used for measurement of low resistance. Derive the conditions for balance. [8M]

   b) An AC bridge has the following constants: [7M]
   Arm AB- Capacitor of 0.5 μF in parallel with 1 kΩ resistance.
   Arm AD- resistance of 2 kΩ.
   Arm DC-Capacitor of 0.5 μF.
   Arm CD-Unknown C_x and R_x in series, frequency 1 kHz.
   Determine the unknown capacitance and dissipation factor.

(OR)

8. a) Explain the theory and working principle of Whetstone's Bridge. Derive the relation for finding unknown resistance. [8M]

   b) With neat sketch explain the basic block diagram of the counter in time interval mode for measuring time interval. [7M]

UNIT-V

9. a) How the transducers are classified on the basis of principle of operation? Discuss. [8M]

   b) With neat diagram explain potentiometer resistance transducer. List advantages and disadvantages. [7M]

(OR)

10. a) With a neat sketch explain LVDT for velocity measurement. [8M]

    b) Explain how to measure temperature? [7M]

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Code No: R1631043 **R16** **SET - 1**

III B. Tech I Semester Supplementary Examinations, June/July-2022

DIGITAL IC APPLICATIONS

(**Common to** ECE, EIE, and E. Comp. E)

Time: 3 hours Max. Marks: 70

Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B)**
2. Answer **ALL** the question in **Part-A**
3. Answer any **FOUR** Questions from **Part-B**

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PART –A (14 Marks)

1. a) Define Fan-in and Fan-out. [2M]
   b) Explain primary constructs VHDL. [2M]
   c) Differentiate between Functions and Procedures in VHDL. [2M]
   d) What are the merits of Look Ahead Carry Generator over Ripple Adder? [3M]
   e) Distinguish between Synchronous and Asynchronous Counters. [3M]
   f) Define state diagram and state table. [2M]

PART –B (56 Marks)

2. a) Give the comparison between TTL and CMOS. Which is better and why? [7M]
   b) List out the Characteristics of ECL? Design a Transistor circuit of 2-input ECL NOR gate, explain the operation with the help of function table? [7M]

3. a) Give the syntax and structure of a Package in VHDL with an example. [7M]
   b) Explain about dataflow design elements of VHDL. [7M]

4. a) Discuss some of the important factors related to synthesis. [7M]
   b) How do you use 'NULL' in a 'case' statement? Can we use 'if' statement in 'case' statement? Explain with examples. [7M]

5. a) Design 5*32 Decoder using one 2*4 decoder and four 3*8 decoders ICs and explain its operation. [7M]
   b) Design a 4×4 combinational multiplier and write VHDL code in dataflow style. [7M]

6. a) Design a ring counter, Johnson counter using 74×194? [7M]
   b) Discuss the logic circuit of 74×377 register and write VHDL program for the same in structural style. [7M]
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7. a) Design an FSM- finite state machine to check whether the two inputs A and B have the same value for the previous three samples. Use Mealy machine for the design. [7M]

   b) Optimize or simplify the following given truth table. Given the input sequence 01010101001. Start from the state *a*, and write the next state and output sequence for both original and optimized tables. [7M]

PS	NS		Output	
	$x = 0$	$x = 1$	$x = 0$	$x = 1$
a	*a*	*b*	0	0
b	*e*	*c*	0	1
c	*a*	*d*	0	1
d	*e*	*f*	0	1
e	*a*	*f*	0	0
f	*g*	*d*	0	1
g	*a*	*b*	0	0

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Code No: R1931041 **R19** **SET - 1**

III B. Tech I Semester Supplementary Examinations, June/July-2022

LINEAR INTEGRATED CIRCUITS AND APPLICATIONS

(Electronics and Communication Engineering)

Time: 3 hours Max. Marks: 75

Answer any **FIVE** Questions **ONE** Question from **Each unit**
All Questions Carry Equal Marks
*****

UNIT-I

1. a) Draw the ac equivalent circuit of single input balanced output differential amplifier and explain its operation. [8M]
   b) List out the various AC characteristics of Op-amp and explain them. [7M]

(OR)

2. a) Draw the circuit diagram of a basic differential amplifier and explain its transfer characteristics. [8M]
   b) Draw the circuit for a 7905 voltage regulator IC and explain its working. [7M]

UNIT-II

3. a) Draw the circuit diagram of an op-amp differentiator and derive an expression for the output in terms of the input. [8M]
   b) Draw the circuit of a voltage to current converter if the load is (i) floating, and (ii) grounded. [7M]

(OR)

4. a) Draw the circuit diagram of an antilogarithmic amplifier using Op-Amps and explain its operation. [8M]
   b) An op-amp is being used as voltage-to-current converter. The value of resistance used in the circuit R is 6.8 kΩ, R_L = 2 kΩ, V_1= 5 V, V_2= 0 V. Determine the values of I_L, V_L and V_o. Draw the circuit. [7M]

UNIT-III

5. a) Design a wide band-reject filter having f_H= 200 Hz and f_L = 1 kHz. Draw the circuit and assume necessary data. [8M]
   b) For the circuit shown, in Fig.1, if R = 22 kΩ and C = 0.01 μF, determine the value of f_c. [7M]

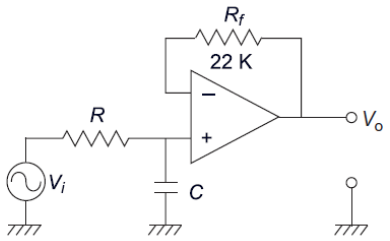

Fig.1

(OR)

6. a) Given a bandpass filter with the component values shown in below Fig.2, find its resonant frequency and bandwidth. [8M]

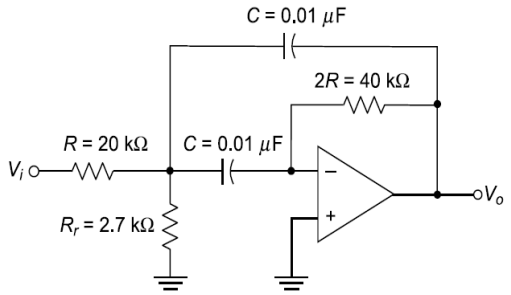

Fig.2

b) Design a second order lowpass Butterworth filter with a cut-off frequency of 12 kHz and unity gain at low frequency. Also determine the voltage transfer function magnitude in dB at 15 Hz for the filter. [7M]

UNIT-IV

7. a) Explain the operation of a Schmitt trigger using IC 555. [8M]
   b) Explain the application of PLL as a frequency multiplier with a neat diagram. [7M]

(OR)

8. a) What is the principle of monostable multivibrator? Explain. [7M]
   b) Draw the block diagram of IC 566 VCO and explain its operation. [8M]

UNIT-V

9. a) Explain the operation of weighted resistor type of DAC with a neat diagram and also write its advantages. [8M]
   b) Explain in detail the operation of 3-bit parallel ADC with a neat circuit diagram. [7M]

(OR)

10. a) Draw the simplified block diagram of a successive approximation ADC and explain its working. [8M]
    b) Explain the differences between current-mode and voltage-mode R–2R ladder D/A converters. [7M]

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Code No: R1631041 **R16** **SET - 1**

III B. Tech I Semester Supplementary Examinations, June/July-2022

COMPUTER ARCHITECTURE AND ORGANIZATION

(Electronics and Communication Engineering)

Time: 3 hours Max. Marks: 70

Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B)**
2. Answer **ALL** the question in **Part-A**
3. Answer any **FOUR** Questions from **Part-B**

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PART –A (14 Marks)

1. a) Write a short note on bus structures used in computer system. [2M]
   b) Give example for left and right shift operations. [2M]
   c) With an example write about Indexed addressing. [2M]
   d) What is the use of Universal Serial bus in a computer system? [3M]
   e) What is the purpose of cache memory? [2M]
   f) Define Microcode. [3M]

PART –B (56 Marks)

2. a) What is System Software? Explain about the System Software of computers. [7M]
   b) Discuss briefly about the history of computer development. [7M]

3. a) An 8-bit register contains the binary value 10011100. What is the register value after arithmetic shift right? Starting from the initial number 10011100, determine the register value after an arithmetic shift left, and state whether there is an overflow? [7M]
   b) What is register transfer notation? Write and explain these notations to three-address, two-address, single address and zero-address instruction types. [7M]

4. What is purpose of Branch Instructions? List out Branch Instructions and write any example program using these Instructions. [14M]

5. a) Explain the importance of handshake control for data transfer in asynchronous bus? [7M]
   b) Explain typical read operation with various data transfer signals on the PCI bus. [7M]
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6. a) What are the possible configurations of ROM? Explain with advantages and disadvantages. [7M]
   b) Discuss briefly how large storage can be implemented with optical disks. [7M]

7. a) Explain, how address sequencing is done in a micro programmed control unit? [7M]
   b) What are the microinstructions needed for the fetch routine? Explain. [7M]

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Code No: RT31042 **R13** SET - 1

III B. Tech I Semester Supplementary Examinations, June/July-2022

LINEAR INTEGRATED CIRCUITS AND APPLICATIONS

(Electronics and Communication Engineering)

Time: 3 hours Max. Marks: 70

Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B)**
2. Answering the question in **Part-A** is compulsory
3. Answer any **THREE** Questions from **Part-B**

*****

PART –A (22 Marks)

1. a) List the characteristics of Amplifiers. [3M]
   b) Draw the block diagram of Op-Amp. [3M]
   c) Draw the circuit of a summing operational amplifier using inverting amplifier configuration. [4M]
   d) Write the applications of Multiplexers. [4M]
   e) What is a VCO? Give two applications that require VCO. [4M]
   f) Explain about basic DAC with a schematic diagram. [4M]

PART –B (48 Marks)

2. a) What is a differential amplifier? Explain about Dual-input Balanced-output differential amplifier. [8M]

   b) The following specifications are given for the DIBO differential amplifier: [8M]
   R_c = 2.2 kΩ, R_E = 4.7 kΩ, $R_{in1} = R_{in2}$ = 50 Ω, V_{CC} = 10 V, $-V_{EE}$ = -10 V and transistor is the CA3086 with $\beta_{dc} = \beta_{ac}$ = 100 and V_{BE} = 0.715 V. Determine:
   (i) the I_{CQ} and V_{CEQ}
   (ii) Voltage gain
   (iii) the input and output resistance

3. a) Draw the block schematic of an Op-Amp and explain the functions of each block. [8M]
   b) The two input terminals of an Op-Amp are connected to voltage signals of strength 645 μv and 740 μv respectively. The gain of the Op-Amp in differential mode is 5×10^5 and its CMRR is 60 dB. Calculate the output voltage and percentage error due to common mode. [8M]

Code No: R1931042 **R19** **SET - 1**

III B. Tech I Semester Supplementary Examinations, June/July-2022

MICROPROCESSORS AND MICROCONTROLLERS

(Electronics and Communication Engineering)

Time: 3 hours Max. Marks: 75

Answer any **FIVE** Questions **ONE** Question from **Each unit**
All Questions Carry Equal Marks
*****

UNIT-I

1. a) What are the functions of Bus Interface Unit (BIU) and Execution Unit (EU) in 8086? [8M]
   b) Define a microprocessor. Explain in detail the evolution of microprocessor in microprocessor age from 4004 MP to core-2 system. [7M]

(OR)

2. a) Evaluate system bus timing with neat block diagram. [8M]
   b) Differentiate between microprocessor unit and microcontroller unit. [7M]

UNIT-II

3. a) Outline the use of the following assembler directives: [8M]
   DD, ASSUME, EQU and LABEL.
   b) Write 8086 program to add the content of one segment to another segment. [7M]

(OR)

4. a) Write 8086 program to find the square root of a perfect square root number. [8M]
   b) Discuss the program development steps and instructions for 8086 programming. [7M]

UNIT-III

5. a) Define DMA. Generalize the concepts of DMA based data transfer using DMA controller. [8M]
   b) How do you interface a seven-segment display? Explain. [7M]

(OR)

6. a) Describe the need for 8259 programmable interrupt controllers. [8M]
   b) With a neat sketch, explain the function of DMA controller. [7M]

UNIT-IV

7. a) With the necessary diagram of control word format, explain the various operating modes of timer in 8051 microcontroller. [8M]
   b) Write the algorithm and ALP for traffic light control system. [7M]

(OR)

8. a) Write a program to multiply the given number 48H and 30H using 8051. [8M]
   b) Explain the stepper motor interface using 8051 microcontroller. [7M]

UNIT-V

9. a) Illustrate the Functional Diagram of ARM Cortex-M3 Processor and explain the development units. [8M]
   b) Describe the loops, subroutines and parameter passing of ARM cortex-M3 programming. [7M]

(OR)

10. a) Describe the special functions and interfaces in ARM processor. [8M]
    b) Discuss the instruction set, system address map and bit banking of programer's model. [7M]

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Code No: R1631042 **R16** **SET - 1**

III B. Tech I Semester Supplementary Examinations, June/July-2022

LINEAR IC APPLICATIONS

(**Common to** Electronics and Communication Engineering, Electronics and Computer Engineering)

Time: 3 hours Max. Marks: 70

Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B)**
2. Answer **ALL** the question in **Part-A**
3. Answer any **FOUR** Questions from **Part-B**

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PART –A (14 Marks)

1. a) What is the purpose of level transistor in differential amplifier? [2M]
   b) What is the importance of gain-bandwidth product of an op-amp? [2M]
   c) What are the practical difficulties associated with the integrator circuit? [2M]
   d) Write the various design steps of second order high pass Butterworth filter. [3M]
   e) Define capture range and lock range in PLL. [3M]
   f) Define conversation time and settling time in ADC and DAC. [2M]

PART –B (56 Marks)

2. a) Explain the transfer characteristics of a differential amplifier pair. [7M]
   b) With suitable circuit diagram, explain the single input balanced output differential amplifier and derive necessary expressions for dc and ac analysis. [7M]

3. a) What is CMRR and slew rate? Explain how CMRR influence the performance of an Op-Amp. [7M]
   b) Explain the bias current compensation technique in an inverting amplifier. [7M]

4. a) Draw the block diagram of a non-linear function generator and explain its operation. [7M]
   b) Draw the instrumentation amplifier and explain its operation in detail. [7M]

5. a) Design a second-order band pass filter with mid-band voltage gain A_o = 50, centre frequency f_o = 160 Hz, and bandwidth = 16 Hz. Draw the circuit. [7M]
   b) Draw the circuit diagram of balanced modulator using IC1496 and explain its operation. [7M]

6. a) Implement a Schmitt trigger circuit using 555 timer and explain the operation using relevant waveforms. [7M]
   b) Draw the block diagram of 555 PLL and explain about each block. [7M]

7. a) Draw the circuit of weighted resistor DAC and derive expression for output analog voltage [7M]
   b) Draw the circuit diagram of counter type ADC and explain its operation in detail. [7M]

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